Si471x Evaluation Board User's Guide

1. Introduction

Thank you for purchasing the Silicon Laboratories Inc. Si471x FM Transmitter Evaluation Board (EVB). This EVB and associated software has been designed to speed the overall development process and decrease the required development time from EVB to product launch. We are looking forward to working with you, and have posted support articles, answers to frequently asked questions, and application notes at www.mysilabs.com.

The Si471x EVB kit should include the following important items:

- Si471x FM Transmitter customer welcome and evaluation letter
- Si471x EVB baseboard Revision 1.3 (Firmware 1.B)
- Si471x daughter card Rev 1.2 with Si471x chip pre-mounted
- EVB characterization report
- Si471x CD including:
  - Development application GUI

2. Overview

The Si471x Evaluation Kit includes an evaluation board (EVB) to facilitate evaluation of the Si471x using the associated software. The EVB consists of a baseboard with a pre-mounted daughter card—Si471x is pre-installed on the daughter card. The Si471x comes in a 3 x 3 mm 20-pin QFN package. Several input/output (I/O) connections provide access to the various subsystems on the EVB. Refer to Figure 1 for the location of the various I/O connectors/devices.

The Si471x family includes:

- Si4710 - FM Transmitter
- Si4711 - FM Transmitter with RDS
- Si4712 - FM Transmitter with Received Power Scan (RPS)
- Si4713 - FM Transmitter with RDS and RPS

This Firmware 1.B release supports Si471x with RDS and limiter as the new feature. On the Si47xx GUI itself, it exposes the overmodulation, loud detection, and silence detection features that have been available from the previous release.

This document references the Si471x data sheet.

Note: The Si471x Firmware 1.B uses library R4, which is not backwards compatible with the Si471x part that uses library R1 (e.g. Alpha 0, Alpha 1, Alpha 2, and Alpha 3).

3. Description

The following sections refer to both the image in Figure 1 and the silkscreen on the Si471x EVB. It is recommended to refer to both when using this guide.

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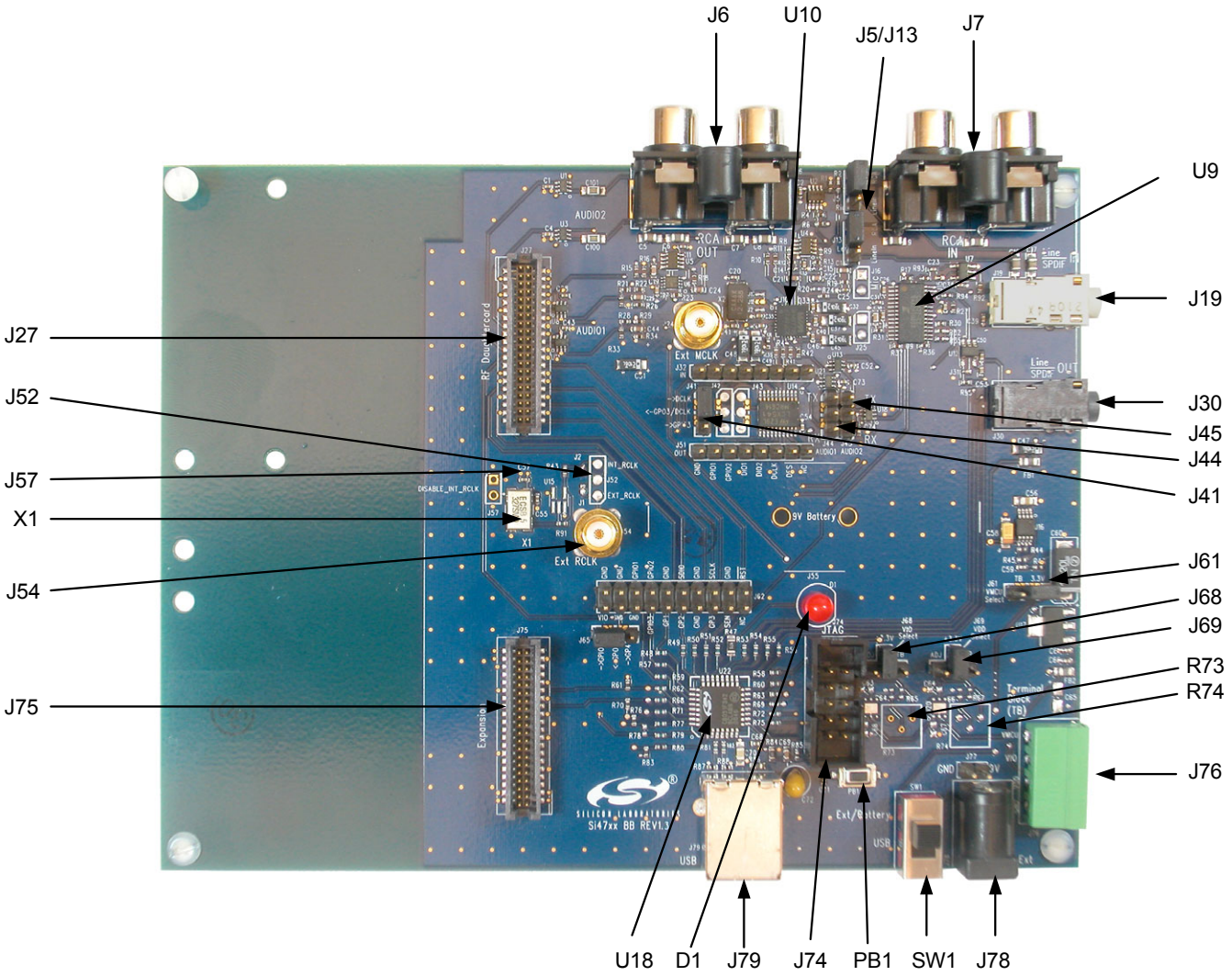

Figure 1. Baseboard Connectors, Jumpers and Devices (Alpha 2)

Baseboard Power Connectors/Devices:

J79 USB connector (using USB power)
J78 External power connector
J76 Terminal block (TB) power connector
SW1 Switch to select between USB power or Ext power
R73 Potentiometer to adjust Vio voltage
R74 Potentiometer to adjust Vdd voltage

J61 Jumper: Baseboard power select (3.3 V or terminal block (TB))
J68 Jumper: Si471x VIO power select (3.3 V or adjustable voltage via R73 or TB)
J69 Jumper: Si471x VDD power select (3.3 V or adjustable voltage via R74 or TB)

Baseboard Audio I/O Connectors/Devices:

J7 RCA input
J6 RCA output
J19 Line/SPDIF input
J30 Line/SPDIF output
U9 S/PDIF Translator
U10 CODEC

J5 Jumper: Analog audio right channel select (RCA or Line In)
J13 Jumper: Analog audio left channel select (RCA or Line In)
J41 Jumper: For GPO3/DCLK pin, select between GPO3 or DCLK
J44 Jumper: Si471x Audio1 select (Transmit or Receive)
J45 Jumper: Si471x Audio 2 select (Transmit or Receive)

Baseboard Clock Connectors/Devices:

X1 32.768 kHz crystal oscillator
J52 Jumper: select Int RCLK or Ext RCLK
J54 Ext RCLK SMA connector input
J57 Jumper: disable Int RCLK

Baseboard MCU Connectors/Devices:

U18 C8051F342 MCU
J79 USB connector to communicate with the MCU
J74 JTAG connector for the MCU
PB1 Push button to reset the MCU
D1 LED to confirm power supply to the MCU

Baseboard to Daughter Board Connectors:

J27 Si471x daughter card connector
J75 Expansion card connector (reserved)

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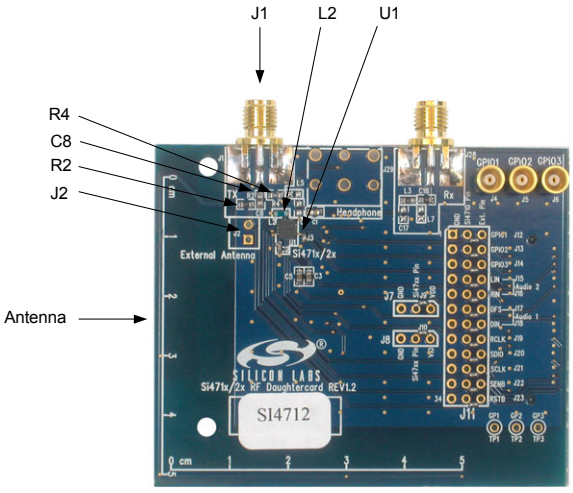

Figure 2. Daughterboard Connectors and Devices

Daughterboard Components:

U1 Si471x FM Transmitter Chip
L2 Tuning Inductor
R2 0 Ω resistor to connect FM TX output to 6cm trace built-in antenna
C8 2 pF capacitor to connect FM TX output to J1 SMA connector
R4 50 Ω terminator resistor
J1 SMA connector for FM transmitter output
J2 Header for putting external antenna

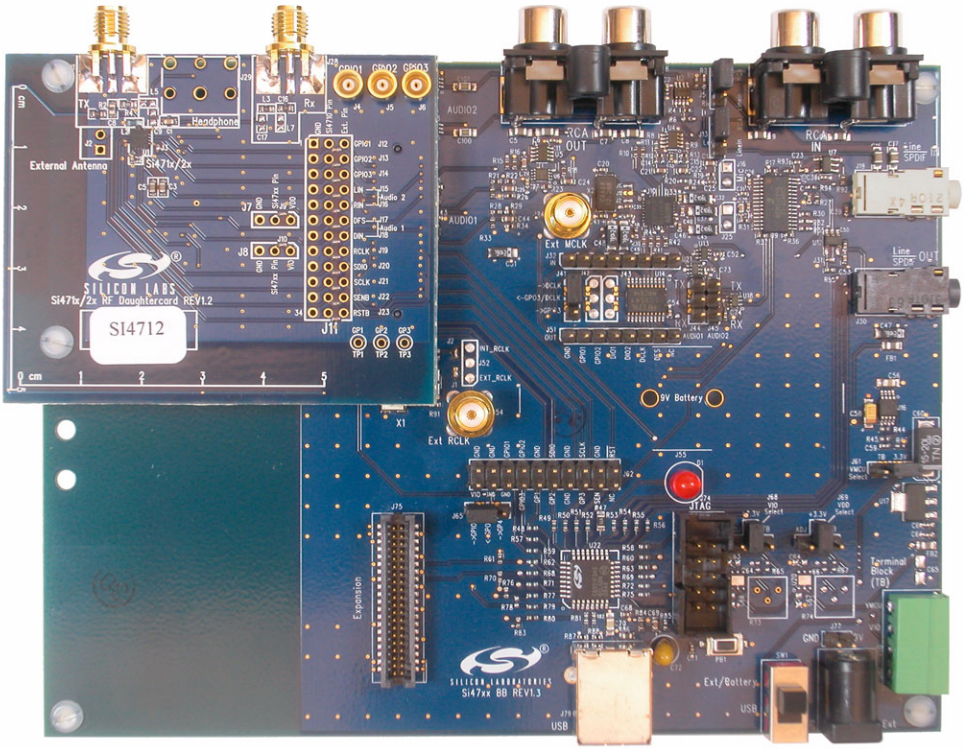

Figure 3. Fully Assembled EVB

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3.1. Jumper or Solder Bump Configuration

The EVB for the Si471x has two different ways to setup jumpers:

1. Berg stick jumper (if the Bergstick headers are installed).
2. Solder bump jumper.

If you have an EVB that doesn't have the header installed, then use the solder bump jumper to select the desired settings. The solder bumps and Bergstick jumpers exist in parallel, so only use one of them. If using the Bergstick jumpers, then remove solder from the solder bumps associated with live Bergstick jumpers. If using the solder bumps, then please make sure there are no jumpers placed on the associated Bergstick jumpers.

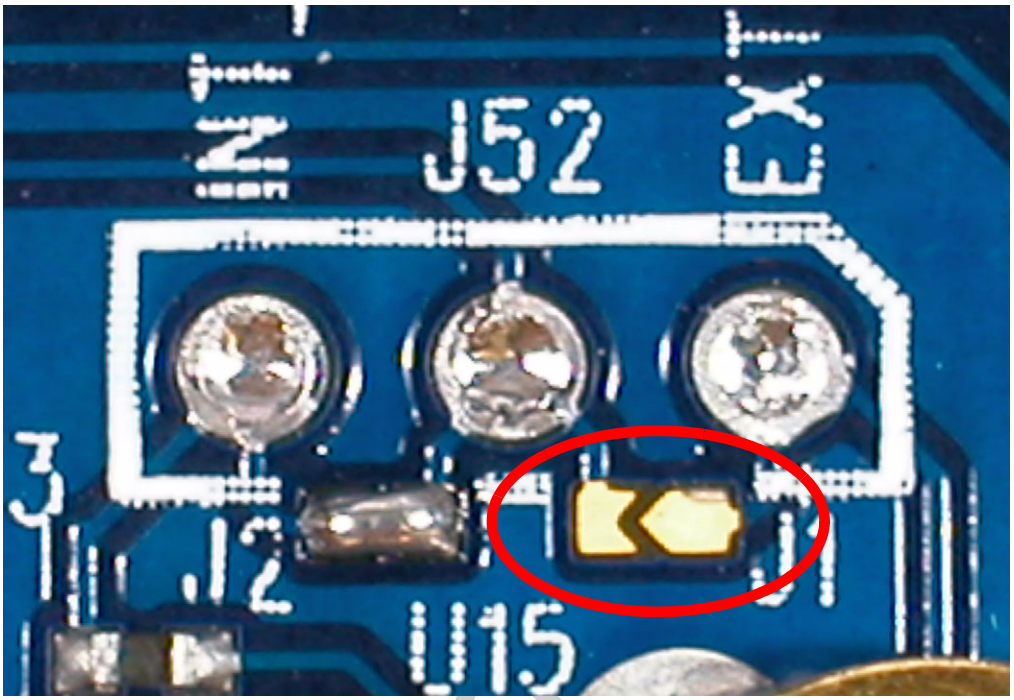

Figure 4. Solder Bump Jumper (circled)

Table 1. EVB Configuration Matrix

Jumper	Description	Choices	Type	Default Setting
J61	Select baseboard power source	+3.3 V/terminal block	Jumper	+3.3 V
J68	Select Vio power source	+3.3 V/terminal block/adjustable via R73	Jumper	+3.3 V
J69	Select Vdd power source	+3.3 V/terminal block/adjustable via R74	Jumper	+3.3 V
J15	Select analog audio in	RCA in/Line in	Jumper	RCA In
J31	Select analog audio in	RCA in/Line in	Jumper	RCA In
J41	Select GPO3 connection	GPIO3/DCLK	Jumper	GPIO3
J44	Select audio 1 configuration	TX/RX	Jumper	RX
J45	Select audio 2 configuration	TX/RX	Jumper	TX
J52	Select RClk source	Int RCLK/Ext RClk	Solder bump	Int RClk
J57	Disable Int RClk	Enable/Disable	Jumper	unconnected (Enable)

3.2. Si471x Base Board

3.2.1. Power Supply Network

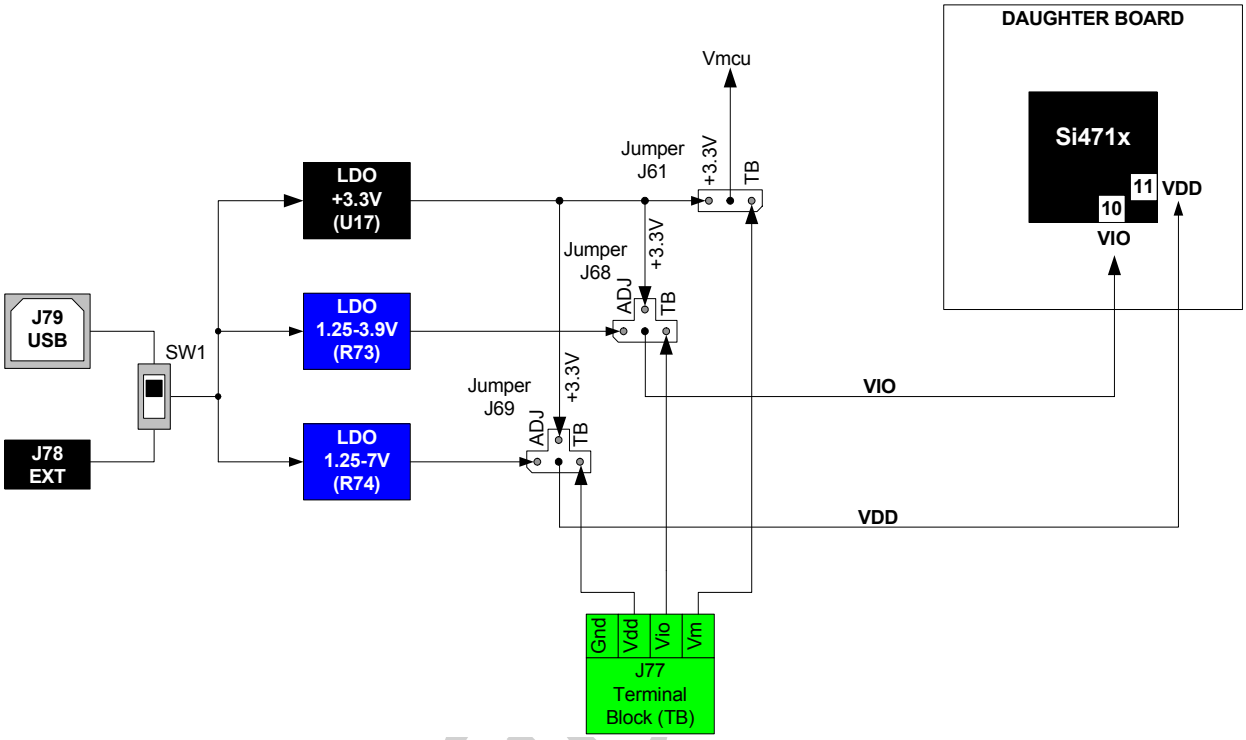

Figure 5. Power Supply Block Diagram

The EVB can be powered from 3 different kinds of power supplies:

1. USB power supply via J79
2. Ext DC power supply via power jack J78
3. Three separate power supplies (Vdd, Vio, Vmcu) via terminal block J76

The EVB has three different rails: Vdd, Vio, and Vmcu. Vdd and Vio are routed directly to the daughter board to power the Vdd and Vio pins on the Si471x chip, while Vmcu is used to power the entire base board.

USB Power Supply & EXT DC Power Supply

Switch SW1 is used to select between the USB supply and Ext DC supply.

There are 2 modes that the user can use with the USB or the EXT DC supply:

1. Fixed +3.3 V
2. Adjustable Vdd and Vio

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Fixed +3.3V

Only one LDO is being used in this mode which outputs a +3.3 V supply to all three Vdd, Vio, and Vmcu supplies. The jumpers need to be set according to Figure 6. This is the default configuration of the EVB.

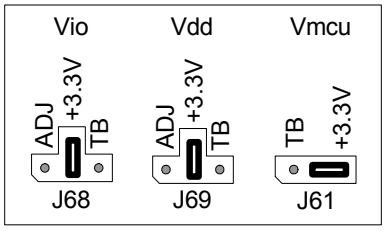

Figure 6. Default Fixed +3.3 V Jumpers Setting

Adjustable Vdd and Vio

In case Vdd and Vio supplies to the Si471x chip need to be adjusted or swept, two adjustable LDOs have been put on the EVB. The Vio supply can be adjusted via potentiometer R73, while Vdd supply via R74. The jumpers need to be set according to Figure 7.

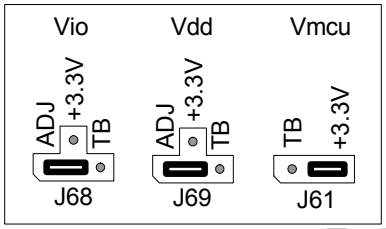

Figure 7. Adjustable Vdd and Vio Jumpers Setting

Terminal Block Power Supply

If the terminal block supplies are used, then jumpers J61, J68 and J69 need to be set to TB according to Figure 8. The user then needs to connect three different power supplies, one each for Vdd, Vio and Vmcu.

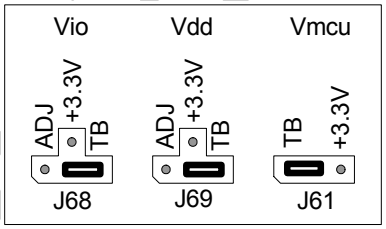

Figure 8. Terminal Block Jumpers Setting

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3.2.2. Microcontroller

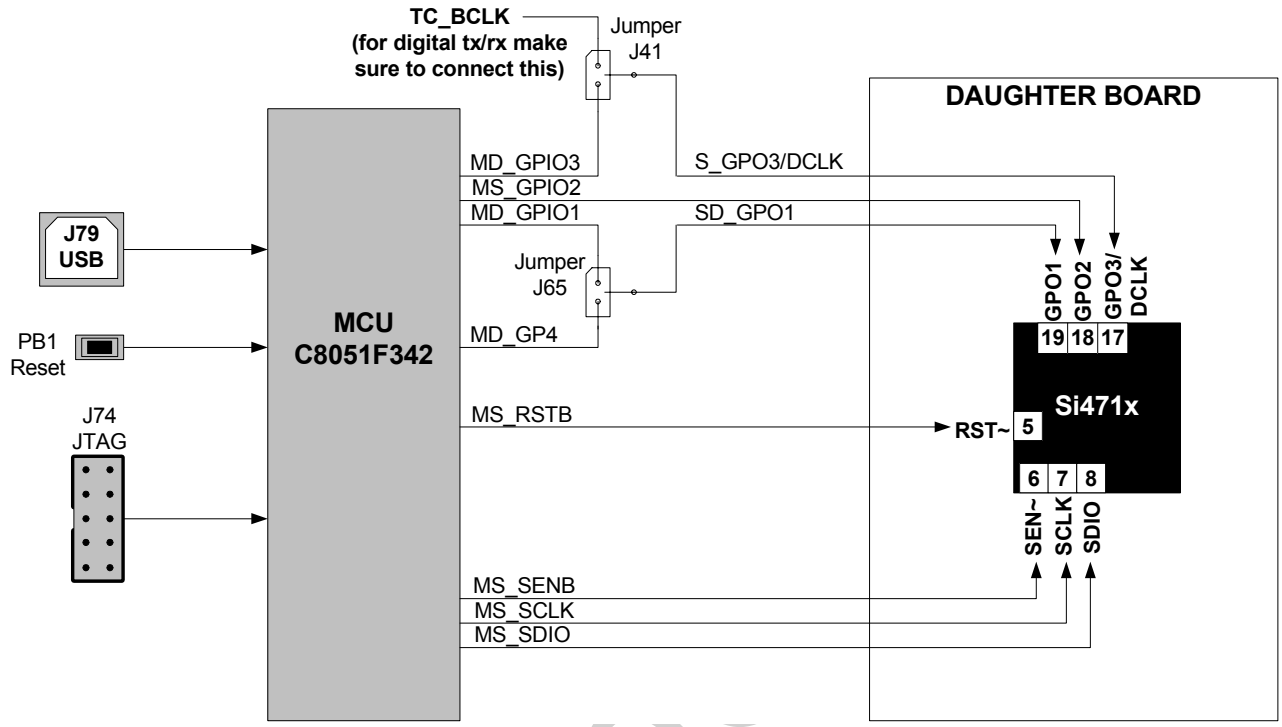

Figure 9. MCU Block Diagram

The Si471x evaluation environment uses a Silicon Laboratories' C8051F342 microcontroller to control the Si471x and to provide USB connectivity to the EVB (via J79). The LED D1 illuminates to confirm that power is being properly supplied to the C8051F342 and that firmware has been loaded. Push-button PB1 manually resets the C8051F342. The JTAG connector J74 is used to program the C8051F342 at production time, and is not necessary for further development.

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3.2.3. Reference Clock for the Si471x

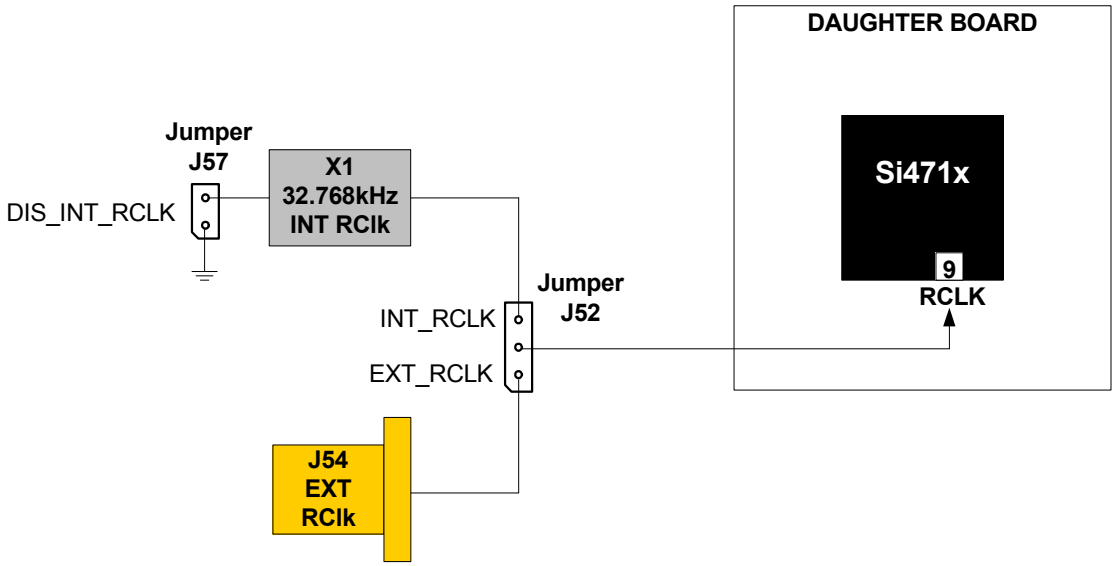

Figure 10. Reference Clock Block Diagram

The Si471x accepts a 32.768 kHz reference clock at the RCLK pin. On the EVB, this clock is provided by a precision crystal oscillator. The user has the option of not using the oscillator and bringing in the reference clock from an external source through SMA connector J54.

When the user chooses to provide an external RCLK jumper J52 has to be set accordingly. Also the user has the option to turn off the onboard crystal oscillator by installing jumper J57.

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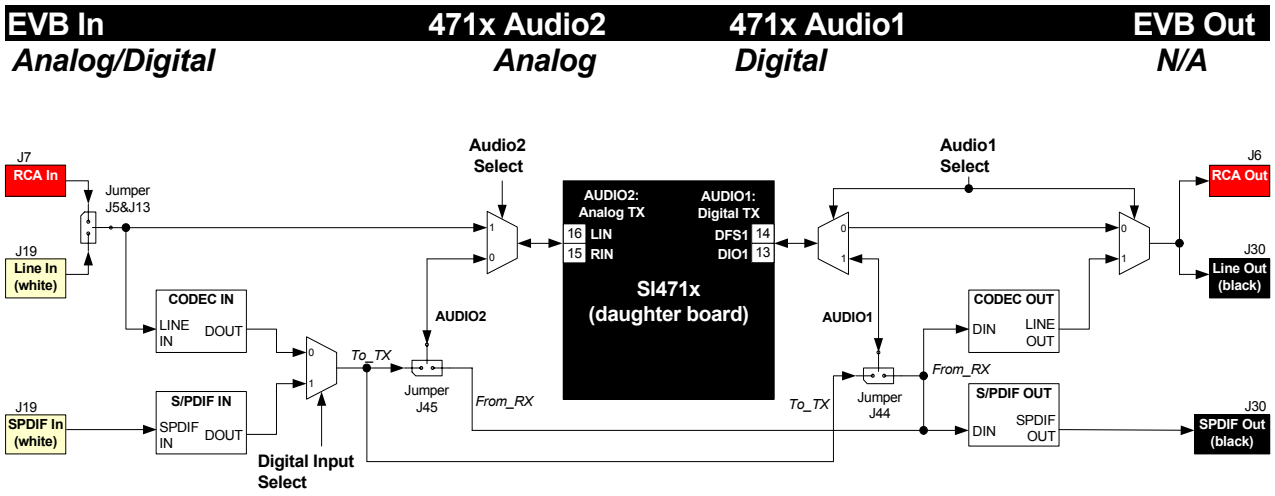
3.2.4. Audio I/O



Note: Jumper J44 and J45 are automatically configured in EVB Rev 1.3.

Figure 11. Audio I/O Block Diagram

The EVB for the Si471x Alpha 3 supports three different kinds of configurations:

1. Analog to Analog
2. Analog to Digital
3. Digital to Digital

Analog to Analog: This configuration provides a way for the user to evaluate the Si471x analog audio input for FM transmission.

The input to the EVB is an analog audio provided via the RCA input connector J7 or LINE In connector J19 (white). Jumpers J5 and J13 are set to RCA input by default. The user has to change this jumper accordingly if LINE In is being used. Then the analog audio input is routed directly through a switch to the Si471x Rin/Lin inputs pin 15 and 16 (Audio2).

Analog to Digital: This configuration provides a way for the user to evaluate the Si471x digital audio input for FM Transmission using an analog audio input.

The input to the EVB is an analog audio provided via the RCA input connector J7 or LINE In connector J19 (white). Jumpers J5 and J13 are set to RCA input by default. The user has to change this jumper accordingly if LINE In is being used. Then the analog audio input is converted by CODEC U10 to a serial audio digital data before it is routed to the Si471x digital audio input DIO and DFS pin 13 and 14 (Audio1). The DCLK input is routed to the GPO3/DCLK pin 17. Make sure that jumper J41 is set to DCLK to ensure proper operation.

Digital to Digital: This configuration provides a way for the user to evaluate the Si471x digital audio input for FM Transmission using an S/PDIF digital audio commonly found in sound cards.

The input to the EVB is a digital S/PDIF data provided via the S/PDIF In connector J19 (white). The digital S/PDIF input is converted by S/PDIF Translator U9 to a serial audio digital data before it is routed to the Si471x digital audio input DIO and DFS pin 13 and 14 (Audio1). The DCLK input is routed to the GPO3/DCLK pin 17. Make sure that jumper J41 is set to DCLK to ensure proper operation.

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IMPORTANT: Jumper Settings

Because of the many possibilities available to configure the EVB, please make sure that these four jumpers are set accordingly:

1. J41: GPO3/DCLK setting
2. J44: TX/RX setting for Audio1 I/O
3. J45: TX/RX setting for Audio2 I/O
4. J5– J13: Analog Audio Source, RCA or Line In

J41: GPO3/DCLK Setting

Upper - DCLK digital audio clock

Lower - GPO3 digital control signal

For configuring the Si471x digital audio input, make

sure that the jumper is set in the Upper position so that the DCLK signal will be routed to the Si471x.

J44: TX/RX setting for Audio1 I/O

Upper - Audio1 is set to FM transmit (pin 13&14 will be the digital audio input).

Lower - Audio1 is set for FM receive (pin 13&14 will be analog/digital audio output).

J45: TX/RX setting for Audio2 I/O

Upper - Audio2 is set to FM transmit (pin 15&16 will be the analog/digital audio input).

Lower - Audio2 is set for FM receive (pin 15&16 will be the digital audio output).

Please refer to the jumper setting instructions found in the Si471x GUI software when configuring the board.

J5–J13: Analog Audio Source, RCA or Line In

Upper - RCA inputs are used for analog audio source.

Lower - Line inputs are used for analog audio source

3.3. Si471x Daughter Card

3.3.1. Si471x FM Transmitter Chip

The Si471x (U1) and its bypass capacitors and tuning inductor (L2) are located on the daughter card. The FM Transmit output can be configured in three different ways:

1. Built-in antenna
2. External antenna
3. RF output

Built-in Antenna

To use the 6 cm trace built-in antenna, please make sure to put a 0ohm resistor in R2 and remove R3 resistor.

External Antenna

To use an external antenna, please remove both R2 and R3 resistors. Put the external antenna in the J2 header connector.

Rf Output

To analyze the performance of the Si471x FM Transmitter Output, please put a 0ohm resistor in R3 and remove R2 resistor. The FM RF output will be available through the SMA connector J1.

Refer to “AN306: Antenna Interface" for a more complete study of the antenna interface for the Si471x.

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4. Recommended Hardware Setup

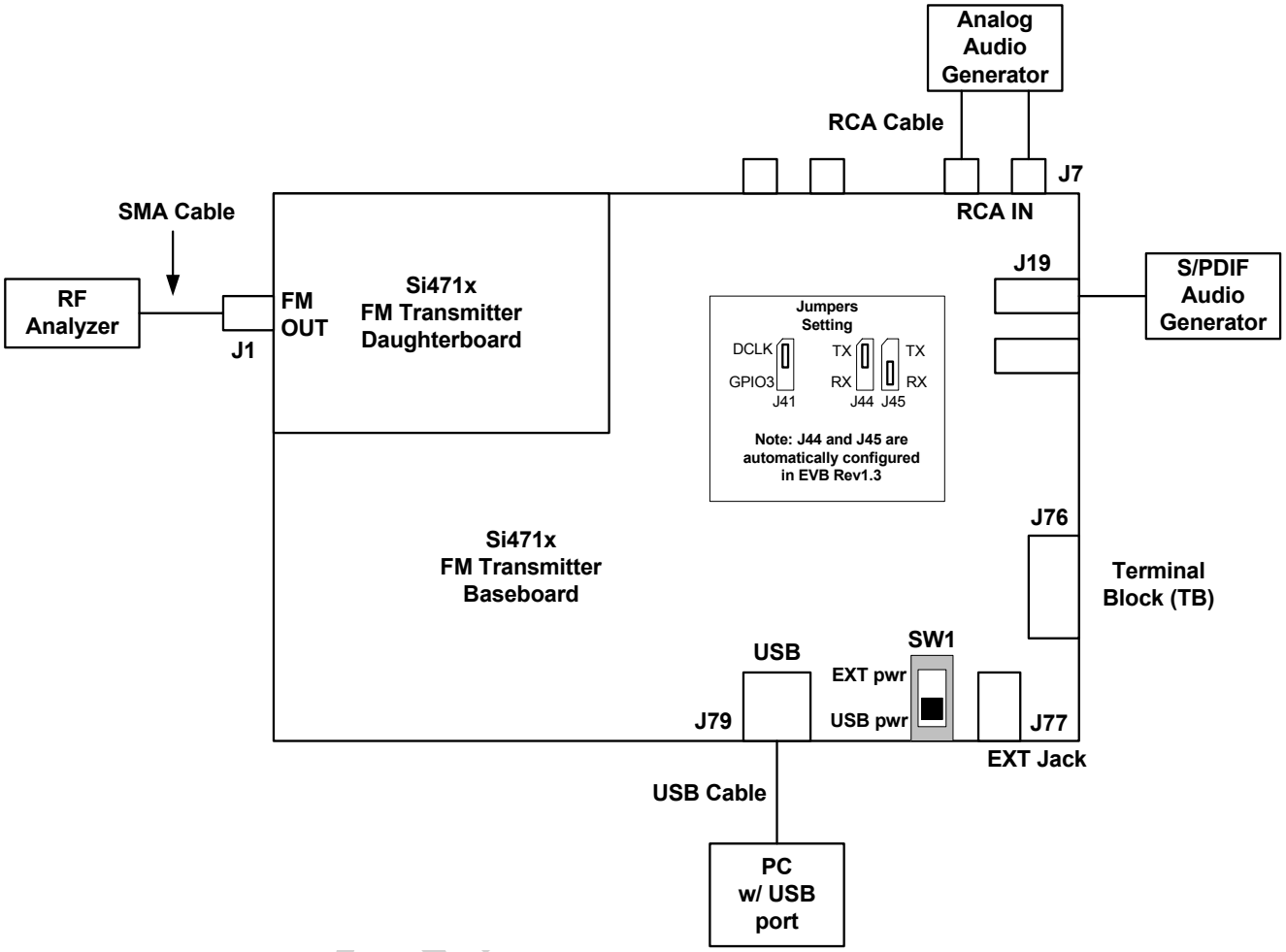

Figure 12. Hardware Setup

Note: The EVB comes with a default jumper configuration that should be ready for evaluating the Si471x.

1. Connect the USB cable from PC to the EVB USB connector J79. The USB connection will serve as a dual purpose: supplying the power to the EVB and controlling the EVB.
2. Connect an analog audio generator to the RCA input connector J7 using an RCA cable or connect an SPDIF digital audio generator to connector J19 using an SPDIF cable.
3. Connect an RF analyzer from the FM output SMA connector J1 using an SMA cable.

5. Getting Started - Software Installation (Firmware 1.B)

The Si471x Windows GUI (graphical user interface) Software is designed and intended for use only with the Si471x evaluation board (EVB). This user guide is written to support Firmware Revision 1.B. The GUI software revision number is available under help\about.

The GUI software development program uses host machine USB port to communicate with the Si471x EVB and is tested for use with Windows XP and Windows 2000.

Note: If you have installed previous version of the GUI, please make sure that:

1. The old version is removed.
2. The Si47xx GUI folder located in "C:\Program Files\Silcon Laboratories Inc" is deleted.

Failure to remove the old version and its folder will cause Si47xx GUI to not function properly.

Below is a couple of screen shots illustrating how to remove the old Si471xx GUI and its folder.

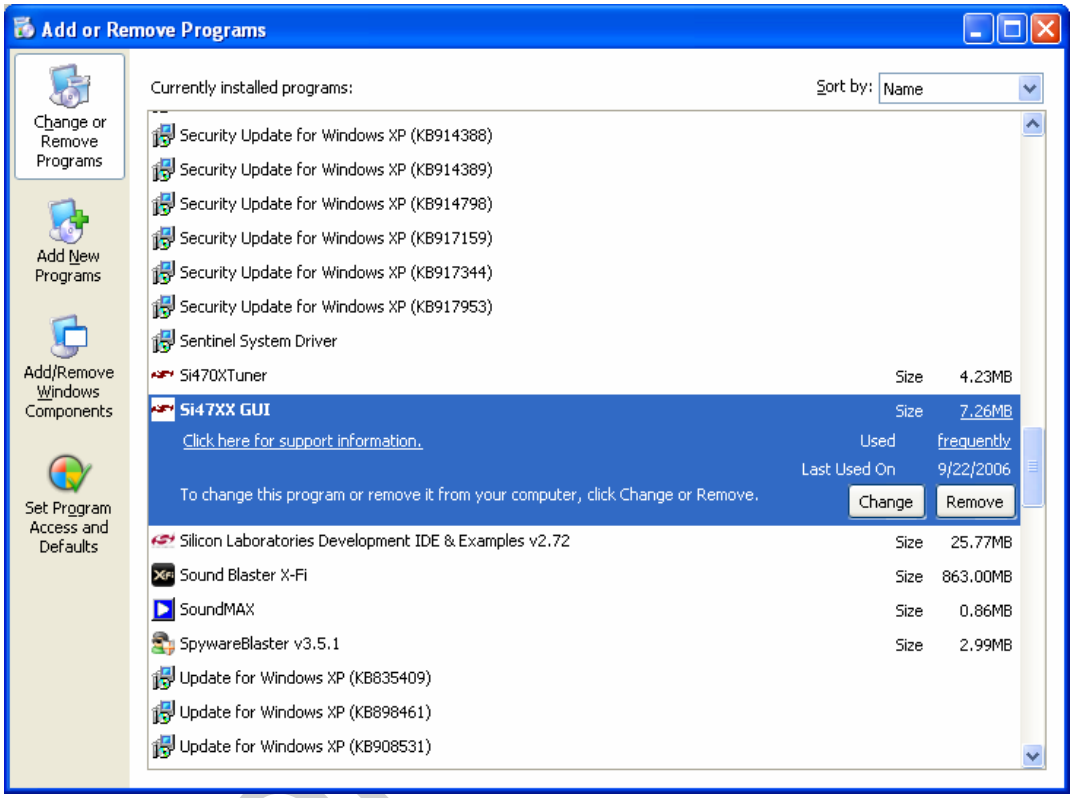
Add or Remove Programs
Change or Remove Programs
Add New Programs
Add/Remove Windows Components
Set Program Access and Defaults
Currently installed programs:
Sort by: Name
Security Update for Windows XP (KB914388)
Security Update for Windows XP (KB914389)
Security Update for Windows XP (KB914798)
Security Update for Windows XP (KB917159)
Security Update for Windows XP (KB917344)
Security Update for Windows XP (KB917953)
Sentinel System Driver
Si470XTuner Size 4.23MB
Si47XX GUI Size 7.26MB
Click here for support information. Used frequently
Last Used On 9/22/2006
To change this program or remove it from your computer, click Change or Remove.
Change
Remove
Silicon Laboratories Development IDE & Examples v2.72 Size 25.77MB
Sound Blaster X-Fi Size 863.00MB
SoundMAX Size 0.86MB
SpywareBlaster v3.5.1 Size 2.99MB
Update for Windows XP (KB835409)
Update for Windows XP (KB898461)
Update for Windows XP (KB908531)

Figure 13. Si47xx GUI Removal

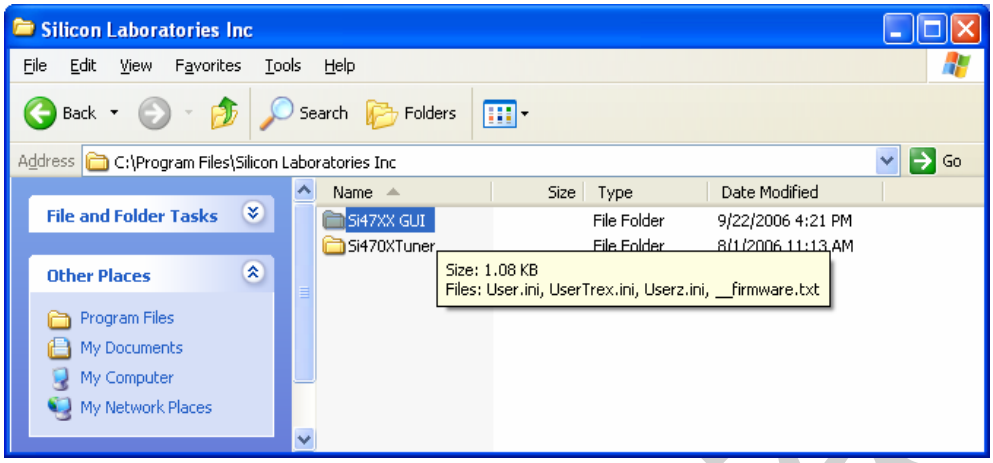

Figure 14. Delete the Si47xx Folder Entirely

After the old version has been removed, insert the Silicon Laboratories, Inc. Si471x CD into the host machine CD drive and launch Windows Explorer. Open the CD to explore the contents in a window like the one shown in Figure 15.

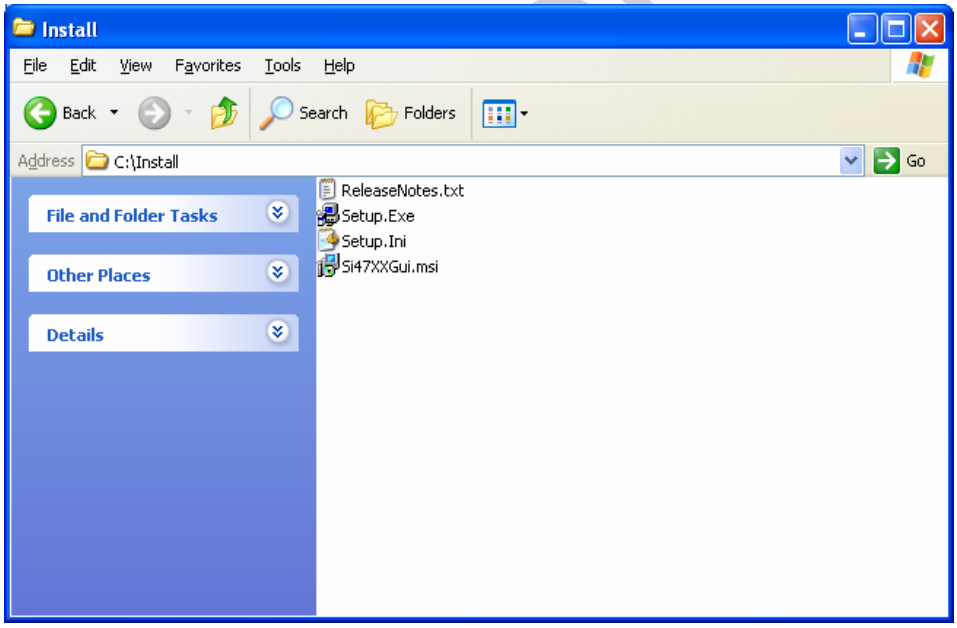

Figure 15. Installation and Setup Start Screen

Important: Open and read the ReleaseNotes.txt file at this point. It may contain information that is not captured here, and which could be very important to the functionality of the EVB or Software.

Run the Setup.Exe and follow the instructions on the screen.

Note: If you get this Error message: "This setup requires the .NET Framework version [1]"; then you should install the .NET Framework that is provided on the CD and re-run the setup.

After installation is finished, an Si47XXGui icon will appear on your desktop. Launch the software by clicking this is icon on the desktop as shown in Figure 16.

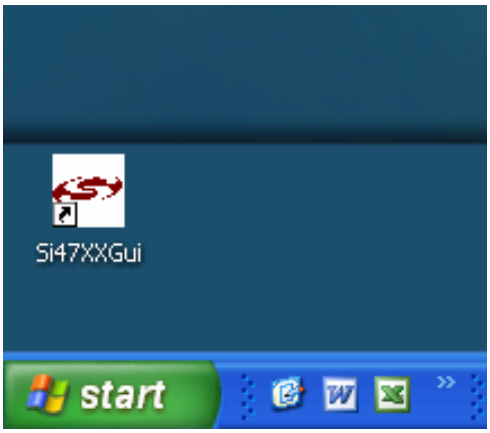

Figure 16. Launching Si471x FM Transmitter Application

The first Si471x window is the Initialization window as shown in Figure 19. Select the target device by clicking on the EVB serial number with the Si471x name underneath. Click open, and a new window displaying "Initializing Transmitter" will appear. There are three modes to configure the Si471x with the Alpha 3 release:

1. Analog Input
2. Analog to Digital Input
3. Digital Input

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5.1. Configuring the Si471x to Receive Analog Input

This mode configures the Si471x to receive analog audio input at pin 15 and 16 (LIN and RIN). The user has the ability to provide analog audio from RCA In connector (J7) or Line In (J19). Please set jumpers J5 and J13 accordingly. Figure 17 shows the configuration setting for analog audio input.

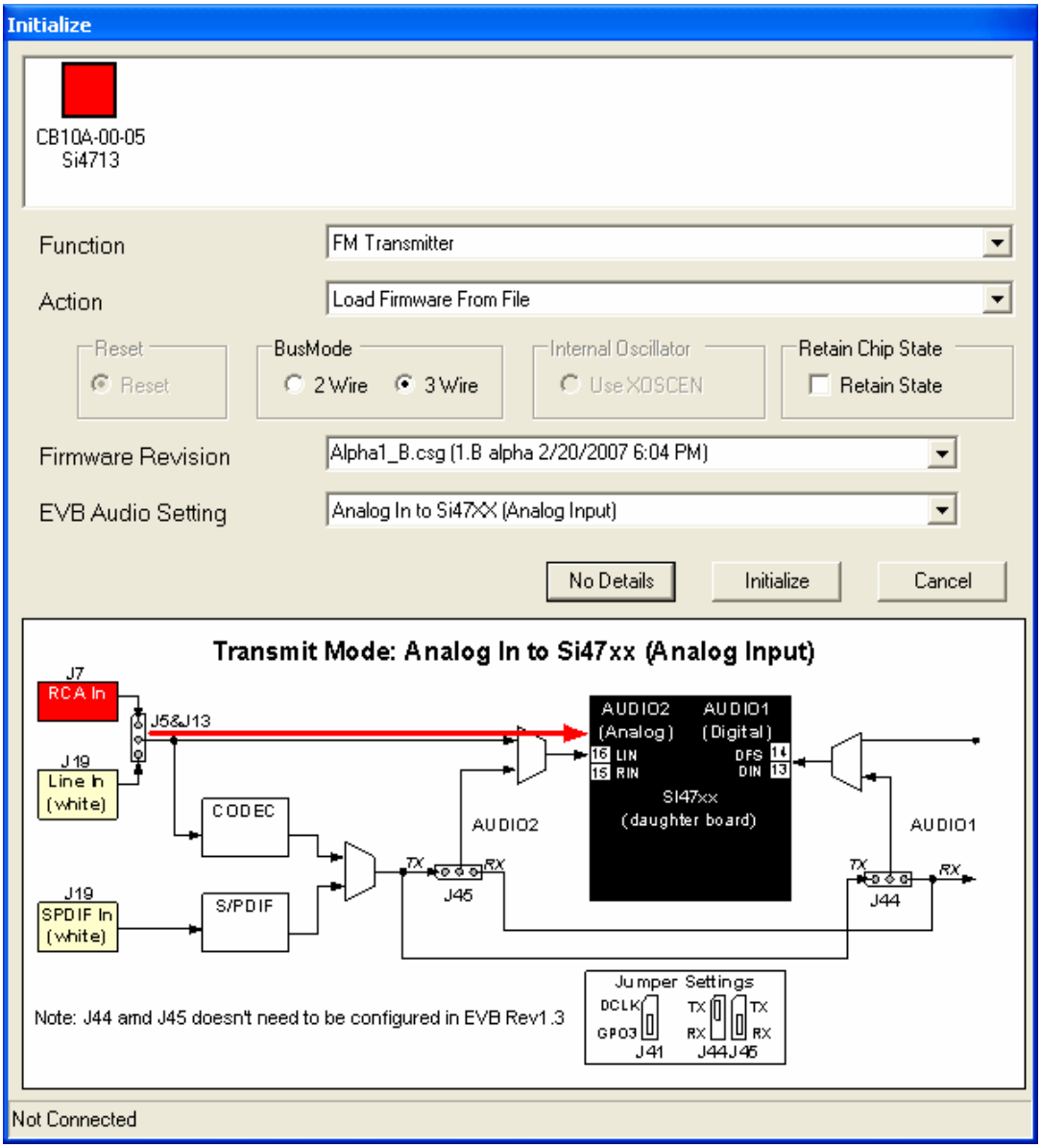

Figure 17. Configuring Si471x to Receive Analog Input

5.2. Configuring the Si471x to Receive Digital Input by Using Analog Source

This mode configures the Si471x to receive digital audio input at pin 13 and 14 (DIN and DFS), but the user still provides an analog audio source to the EVB. It is useful for a user who wants to test digital input on the Si471x but does not have a digital audio source. The analog audio source is converted to digital audio through the CODEC, which can be configured to output various digital audio formats. Please refer to Figure 23, “CODEC Property Window,” on page 25 to control the CODEC.

Note: Please set jumper J41, J44, and J45 according to Figure 18 to properly operate in digital mode.

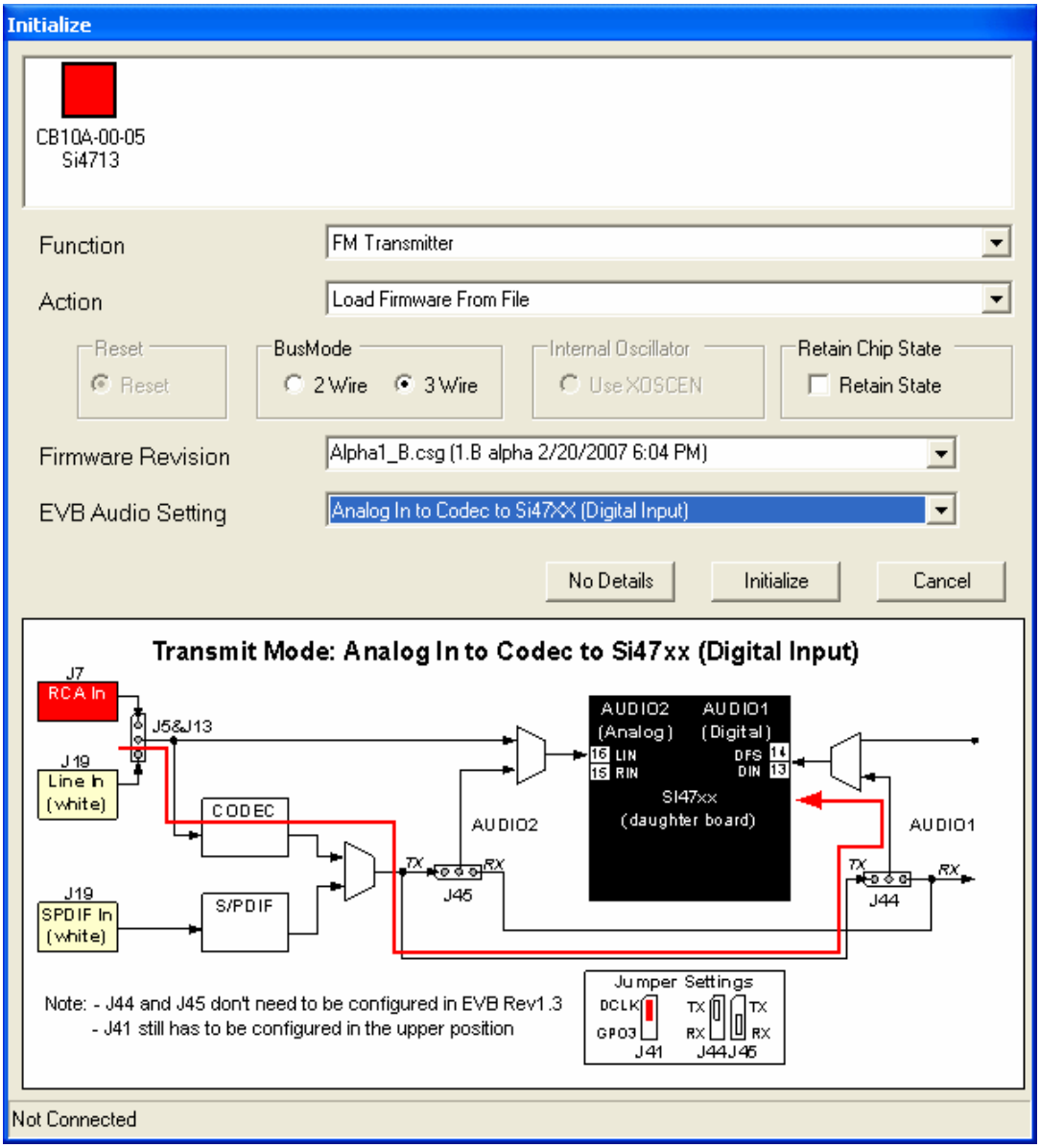

Figure 18. Configuring Si471x to Receive Digital Input by Using Analog Source

5.3. Configuring the Si471x to Receive Digital Input by Using Digital Source (SPDIF)

This mode configures the Si471x to receive digital audio input at pin 13 and 14 (DIN and DFS) when the user has an SPDIF digital audio source. The SPDIF source is converted to PCM digital audio by the SPDIF translator. Please refer to Figure 24, “SPDIF Property Window,” on page 26 to control the SPDIF translator.

Notes: - Please set jumper J41, J44, and J45 according to Figure 19 to properly operate in digital mode.

- The Si471x requires the digital audio signal to be present when initializing the part. Therefore, please connect the SPDIF IN signal prior to initializing the part.

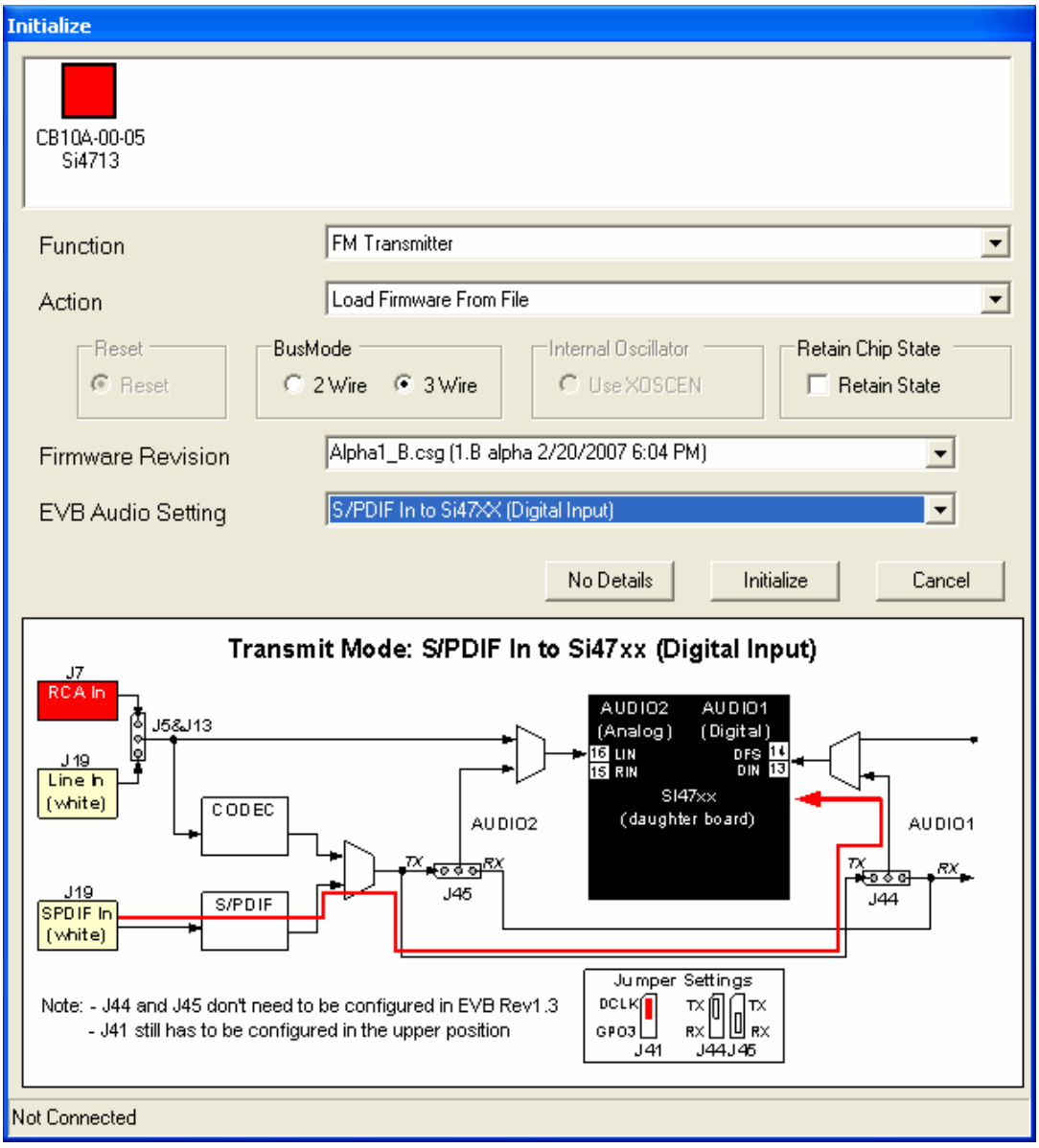

Figure 19. Configuring Si471x to Receive Digital Input by Using Digital Source (SPDIF)

TIP. If the Si471x Development GUI doesn't find your device, try unplugging and plugging in the USB cable again.

6. Development Using Si471x GUI (Firmware 1.B)

6.1. Si47xx GUI - Main Window

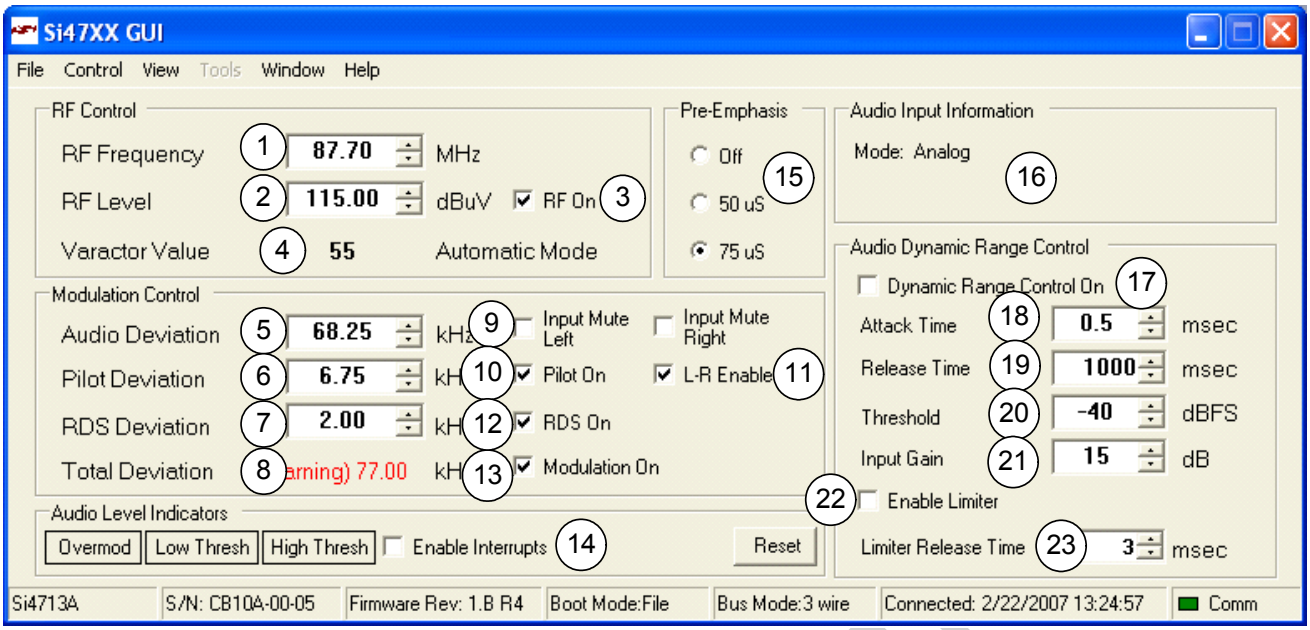

Figure 20. Si471x FM Transmitter Window

Table 2. Control Bit Explanations

#	Explanation	Range
1	Transmit frequency display. Enter the desired FM transmit frequency in this window.	76–108 MHz
2	Transmit power display. Enter the desired FM transmit power in this window.	88–120 dBuV
3	RF on or off. Turning this button on will enable the FM transmit, while turning this button off will disable the FM transmit.	On/Off
4	Varactor Value. This is an indicator showing the tuning cap value of the Si471x chip. Each number represents 0.25 pF. If the varactor value is manually overwritten in the property window, the indicator will change from automatic mode to manual mode.	1–191
5	Audio Deviation. Enter the desired audio deviation in this window.	0–90 kHz
6	Pilot Deviation. Enter the desired pilot deviation in this window.	0–90 kHz
7	RDS Deviation. Enter the desired RDS deviation in this window (Si4711/13 only).	0–7.5 kHz
8	Total Deviation. This is an indicator only displaying the sum of the audio, pilot and RDS deviation. If the total deviation exceeds 75 kHz, the indicator will turn red and a warning sign is displayed.	0–187.5 kHz
9	Input Mute Left/Right. Turning this button will mute the Left or Right audio channel.	On/Off
10	Turn on or off the pilot tone for stereo or mono FM transmit mode.	On/Off
11	Turn on or off the L-R channel for stereo or mono FM transmit mode.	On/Off
12	Turn on or off the RDS transmission (Si4711/13 only).	On/Off
13	Modulation On. Clicking this button on will modulate the audio, pilot, and RDS signal according to the audio, pilot, and RDS deviation. Turning this button off will turn off modulation for all audio, pilot, and RDS signal.	On/Off

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Table 2. Control Bit Explanations (Continued)

#	Explanation	Range
14	Audio Level Indicators: Overmodulation, Audio input level below low-level threshold (silence detection), and Audio input level below high-level threshold (loud detection). To enable these three indicators please check off the Enable Interrupts box. These three indicators are sticky bit, in order to clear these bits, press the Reset button.	—
15	Pre-Emphasis. Click one of the three buttons to set the pre-emphasis either to Off, 50 us or 75 us.	Off, 50 us, 75 us
16	Si471x EVB audio input setting indicator: Analog In / Digital (Analog In to CODEC) / Digital (SPDIF)	Analog, Digital CODEC, Digital SPDIF
17	Turn on or off the compressor for the audio signal	On/Off
18	Attack time. Set the attack time for the compressor in millisecond	0.5–5 ms
19	Release time. Set the release time for the compressor in millisecond	100–1000 ms
20	Threshold. Set the threshold for the compressor	–40 to 0 dBFS
21	Input Gain. Set the compressor gain.	0 to 20 dB
22	Turn on or off the limiter feature	On/Off
23	Set the limiter release time constant	0.5,1,2,3,4,5,6,7,8, 9,10,20,30,40,50, 75,100 ms

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6.2. Si47xx GUI - Analog Property Window

This Analog Property Window controls the various analog audio input properties on the Si471x. Clicking on Windows→Properties when in Analog Mode will launch the Analog Property Window as shown in Figure 21.

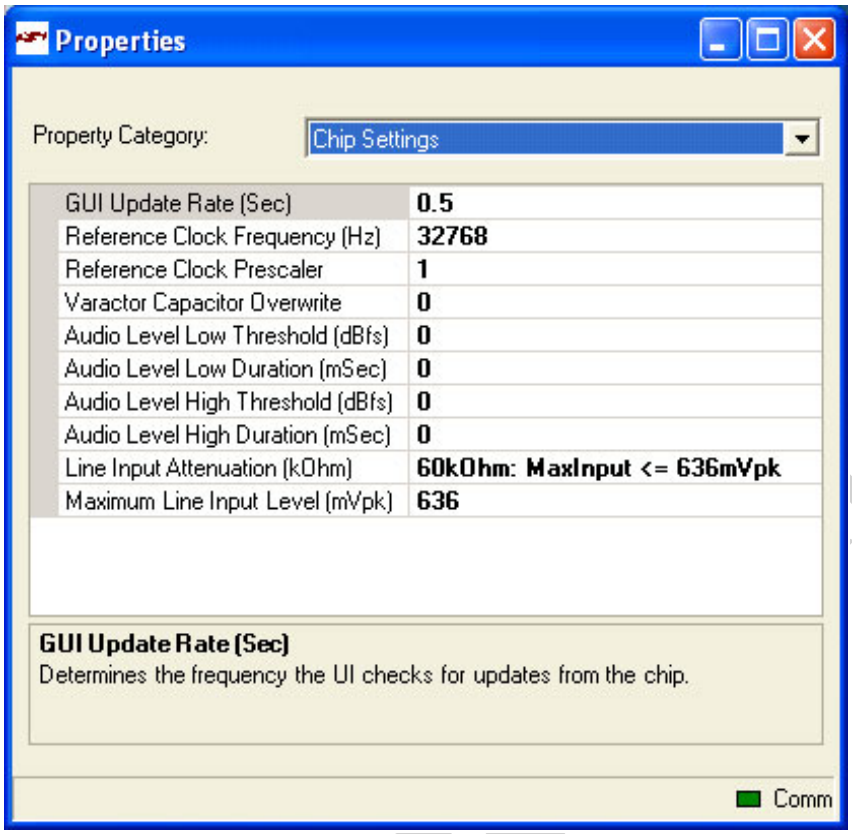

Figure 21. Si471x Analog Property Window

Table 3. Analog Property Window Explanations

Item	Explanation	Range
GUI Update Rate (Sec)	Set the GUI update rate between the computer and the EVB.	0.2–10 Sec
Reference Clock Frequency	This is the internal Reference Clock Frequency on the chip and it is calculated by dividing RCLK by the prescaler.	31130–34406 Hz
Reference Clock Prescaler	Reference Clock Prescaler allow the user to have an RCLK from 32 kHz to 40 MHz. Any RCLK that the user supplies should be divided by this prescaler to get as close to 32.768 kHz as possible.	1–4095
Varactor Capacitor Overwrite	This field allows the user to manually overwrite the tuning capacitance. 0 indicates that the tuning cap is automatically adjusted. Any number other than 0 (1 to 191) will indicate that the tuning cap is manually adjusted.	automatic: 0, manual: 1–191
Audio Level Low Threshold (dBFS)	Set the threshold in which an interrupt will be generated when the audio input level falls below this threshold for the duration greater than the Audio Level Low Distortion setting. This may be called silence detection indicator	–70 to 0
Audio Level Low Duration (mSec)	Set the duration for the audio level low before an interrupt is generated.	0–65535

Table 3. Analog Property Window Explanations (Continued)

Item	Explanation	Range
Audio Level High Threshold (dBFS)	Set the threshold in which an interrupt will be generated when the audio input level rises above this threshold for the duration greater than the Audio Level High Duration setting. This may also be called loud detection indicator.	–70 to 0
Audio Level High Duration (mSec)	Set the duration for the audio level high before an interrupt is generated.	0–65535
Line Input Attenuation	The Si471x chip has 4 attenuator setting (636, 416, 301, and 190 mVp). It will tell the maximum audio input signal that the user can give to the LIN and RIN input. The attenuator setting will determine the audio input impedance (LIN and RIN) of the chip.	190 mVp, 301 mVpk, 416 mVp, 636 mVpk
Maximum Line Input Level	The maximum line input level is like a fine adjustment of the max audio input signal that the user supply to the chip. This number has to be less than or equal to the attenuation setting. The max line input level will correspond to the max audio deviation set in the audio deviation window on the main GUI. Make sure that the actual audio input signal does not exceed this limit, otherwise the audio signal will become distorted.	0–636 mVpk

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6.3. Si47xx Digital Property Window

This Digital Property Window controls the various digital audio input properties on the Si471x. Clicking on Windows→Properties when in Digital Mode will launch the Digital Property Window as shown in Figure 22.

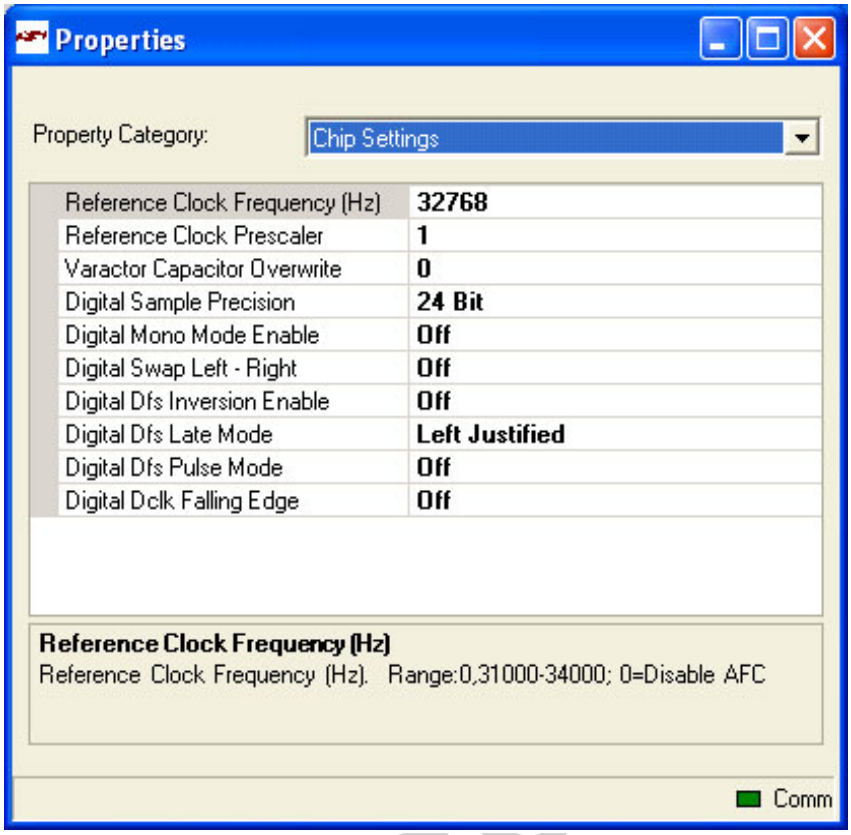
Properties
Property Category:
Chip Settings
Reference Clock Frequency (Hz) 32768
Reference Clock Prescaler 1
Varactor Capacitor Overwrite 0
Digital Sample Precision 24 Bit
Digital Mono Mode Enable Off
Digital Swap Left - Right Off
Digital Dfs Inversion Enable Off
Digital Dfs Late Mode Left Justified
Digital Dfs Pulse Mode Off
Digital Dclk Falling Edge Off
Reference Clock Frequency (Hz)
Reference Clock Frequency (Hz). Range:0,31000-34000; 0=Disable AFC
Comm

Figure 22. Si471x Digital Property Window

Table 4. Si471x Digital Property Window Explanations

Item	Explanation	Range
Reference Clock Frequency	This is the internal Reference Clock Frequency on the chip and it is calculated by dividing RCLK by the prescaler.	31130–34406 Hz
Reference Clock Prescaler	Reference Clock Prescaler allow the user to have an RCLK from 32 kHz to 40 MHz. Any RCLK that the user supplies should be divided by this prescaler to get as close to 32.768 kHz as possible.	1–4095
Varactor Capacitor Overwrite	This field allows the user to manually overwrite the tuning capacitance. 0 indicates that the tuning cap is automatically adjusted. Any number other than 0 (1 to 191) will indicate that the tuning cap is manually adjusted.	automatic: 0, manual: 1–191
Digital Sample Precision	Select the precision of the digital audio input	8, 16, 20, 24 bits
Digital Mono Mode Enable	Select between Digital Stereo or Mono	On/Off
Digital Swap Left - Right	Select whether the DIN L-R data is normal or swapped	On/Off

Table 4. Si471x Digital Property Window Explanations (Continued)

Item	Explanation	Range
Digital DFS Inversion Enable	Select whether the DFS Frame Clock is normal or inverted	On/Off
Digital DFS Late Mode	Select PCM digital audio data between I^2S or Left Justified	On: Left-Justified, Off: I^2S
Digital DFS Pulse Mode	Select between using a regular 50% duty cycle Frame Clock, or a Pulse Frame Clock	On/Off
Digital DCLK Falling Edge	Select between using rising edge or falling edge of DCLK when sampling Digital Input (DIN) data	On/Off

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6.4. Si47xx GUI - CODEC Property Window

This CODEC Property Window controls the various properties of the CODEC on the EVB baseboard. In the Digital Mode, when using the Analog In to CODEC method, the Digital Property Window has a baseboard setting that can be selected in the property category pull-down menu where the window will become the CODEC Property Window.

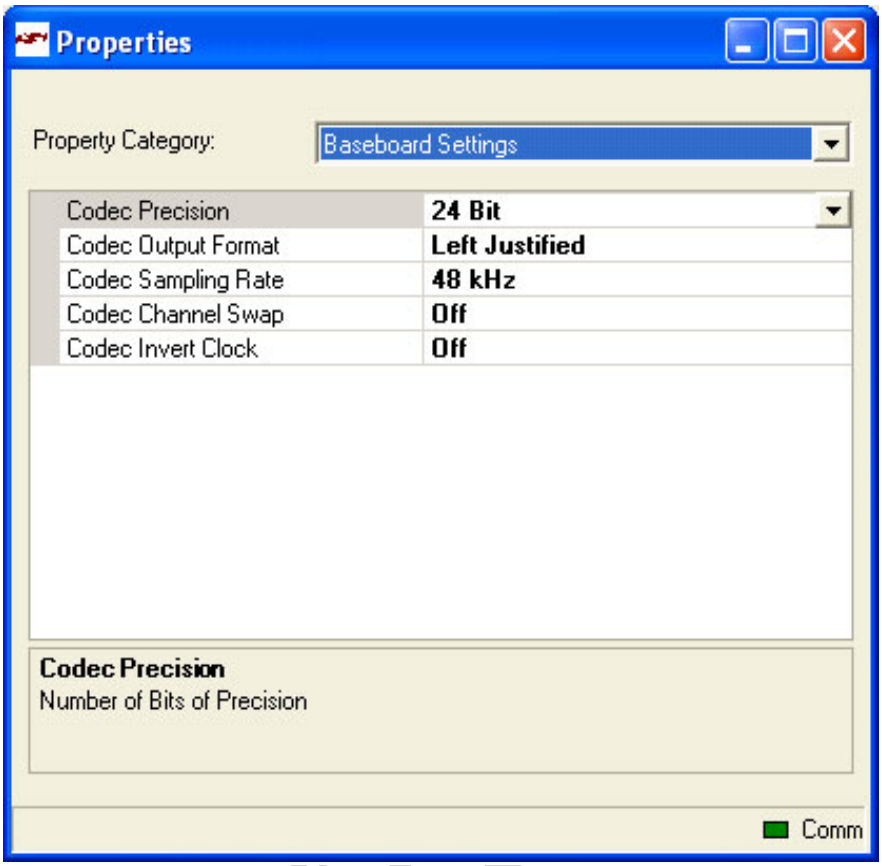

Figure 23. CODEC Property Window

Table 5. CODEC Property Window Explanations

Item	Explanation	Range
CODEC Precision	Select the CODEC digital audio output precision	16, 20, 24 bits
CODEC Output Format	Select the CODEC digital audio format between I^2S or Left Justified	Left-Justified or I^2S
CODEC Sampling Rate	Select the precision of the CODEC digital audio output	32 or 48 kHz
CODEC Channel Swap	Select whether the CODEC digital output L-R data is normal or swapped	On / Off
CODEC Invert Clock	Select between using rising edge or falling edge of DCLK when sampling Digital Input (DIN) data	On / Off

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6.5. Si47xx GUI - SPDIF Property Window

This SPDIF Property Window controls the various properties of the SPDIF translator on the EVB baseboard. In the Digital Mode, when using the SPDIF method, the Digital Property Window has a baseboard setting that can be selected in the property category pull-down menu where the window will become the SPDIF Property Window.

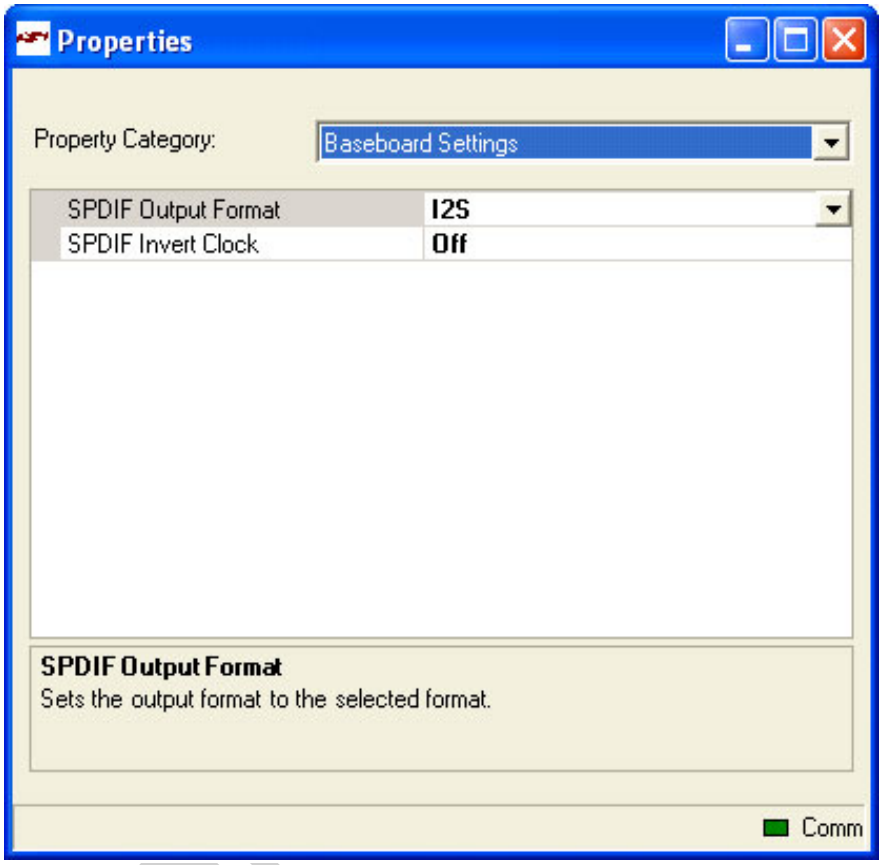

Figure 24. SPDIF Property Window

Table 6. SPDIF Property Window Explanations

Item	Explanation	Range
SPDIF Output Format	Select the SPDIF digital audio format between I^2S or Left Justified	Left-Justified or I^2S
SPDIF Invert Clock	Select between using rising edge or falling edge of DCLK when sampling Digital Input (DIN) data	On / Off

6.6. Si47xx GUI - Register Map Window

The register map window allows the user to manually program the device by sending commands to the chip. Refer to “AN305: Si4710/11 FM Transmitter Programming Guide” to be able to manually program the device. Clicking on Windows→Register Map will launch the Register Map Window as shown in Figure 25.

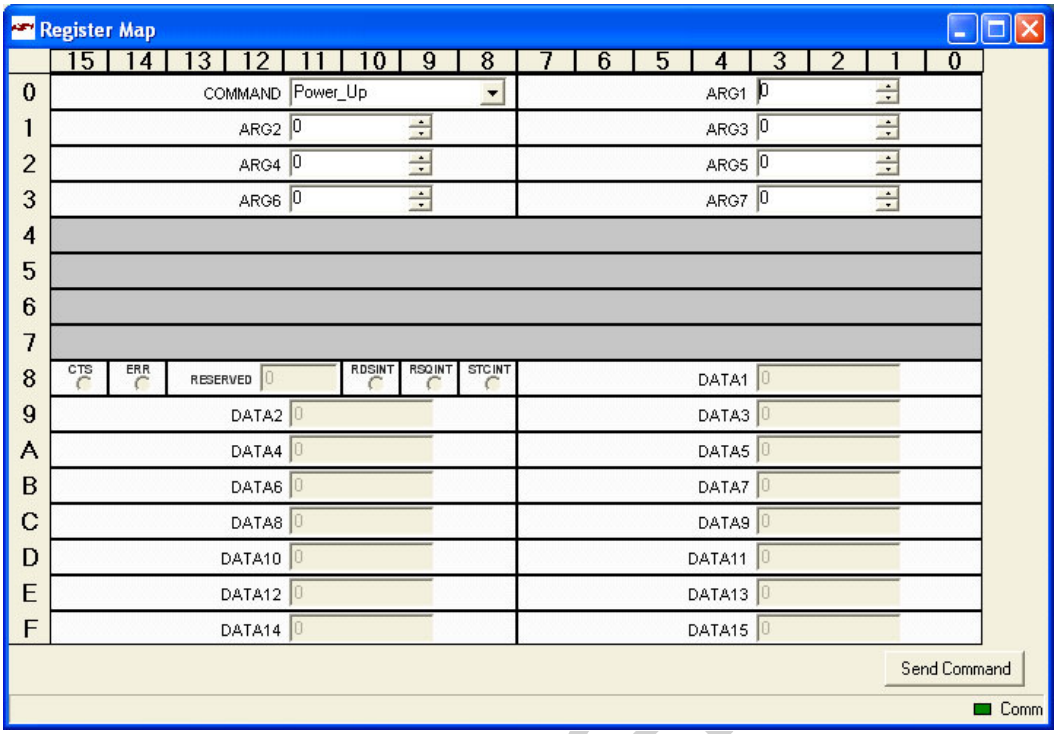
Register Map
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 COMMAND Power_Up ARG1 0
1 ARG2 0 ARG3 0
2 ARG4 0 ARG5 0
3 ARG6 0 ARG7 0
4
5
6
7
8 CTS ERR RESERVED 0 RDSINT RSQINT STCINT DATA1 0
9 DATA2 0 DATA3 0
A DATA4 0 DATA5 0
B DATA6 0 DATA7 0
C DATA8 0 DATA9 0
D DATA10 0 DATA11 0
E DATA12 0 DATA13 0
F DATA14 0 DATA15 0
Send Command
Comm

Figure 25. Si471x Register Map Window

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6.7. Si47xx GUI - Received Power Scan Window

The Received Power Scan Window is only available with the Si4712/13 devices. It enables the user to scan the entire FM band to find an empty channel. The frequency of this channel can then be used to transmit. Clicking on Windows→Power Scan will launch the Received Power Scan Window as shown in Figure 26

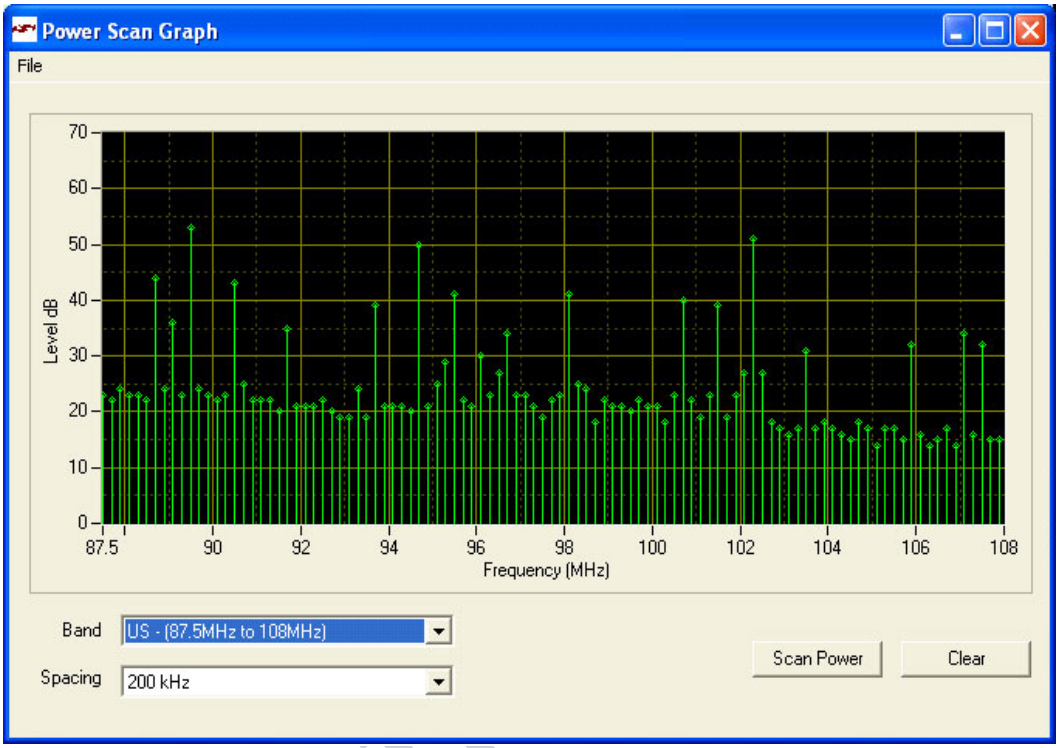

Figure 26. Si4712/13 Received Power Scan Window

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6.8. Si47xx GUI - Radio Data Service (RDS) Window

The RDS/RBDS feature is only available in the Si4711/13 part and the Si47xx GUI allows user to evaluate the RDS/RBDS transmission on these parts. This user guide assumes that the user is already familiar with the RDS/RBDS standard.

User may refer to the following documents if needs to be familiar with the RDS/RBDS standard:

1. United States RBDS Standard by National Radio Systems Committee, April 9, 1998.
2. RDS Universal Encoded Communication Protocol Version 5.1 by European Broadcasting Union, August 1997.
3. Silicon Labs AN243: Using RDS/RBDS with the Si4701/03

In order for the user to transmit RDS please check the RDS On box. Failure to turn on RDS means that the RDS data will not be transmitted. The following picture illustrated the RDS On box that should be turned on.

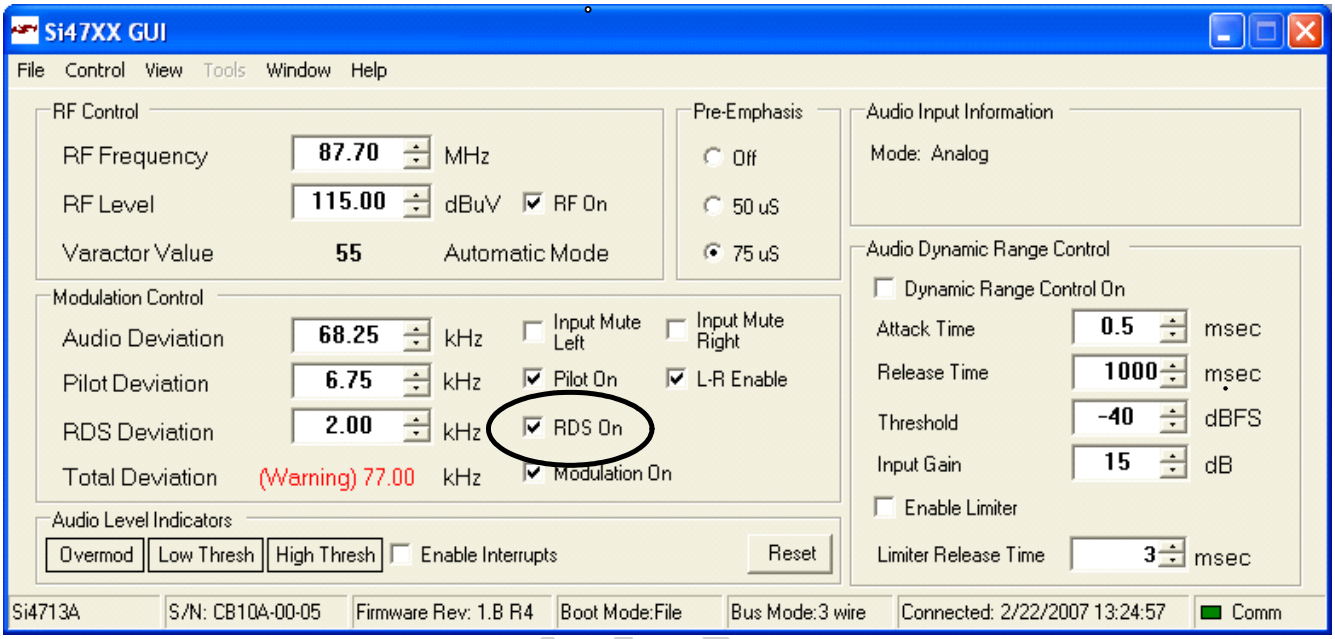

Figure 27. Turning on RDS in the Main GUI Window

After the RDS transmission is enabled, click on Window -> RDS Transmit Data to go to the RDS Transmit Data screen. This window allows the user to play around with what kind of RDS data will be transmitted and also allows the user to gain insight to the Si471x RDS capability.

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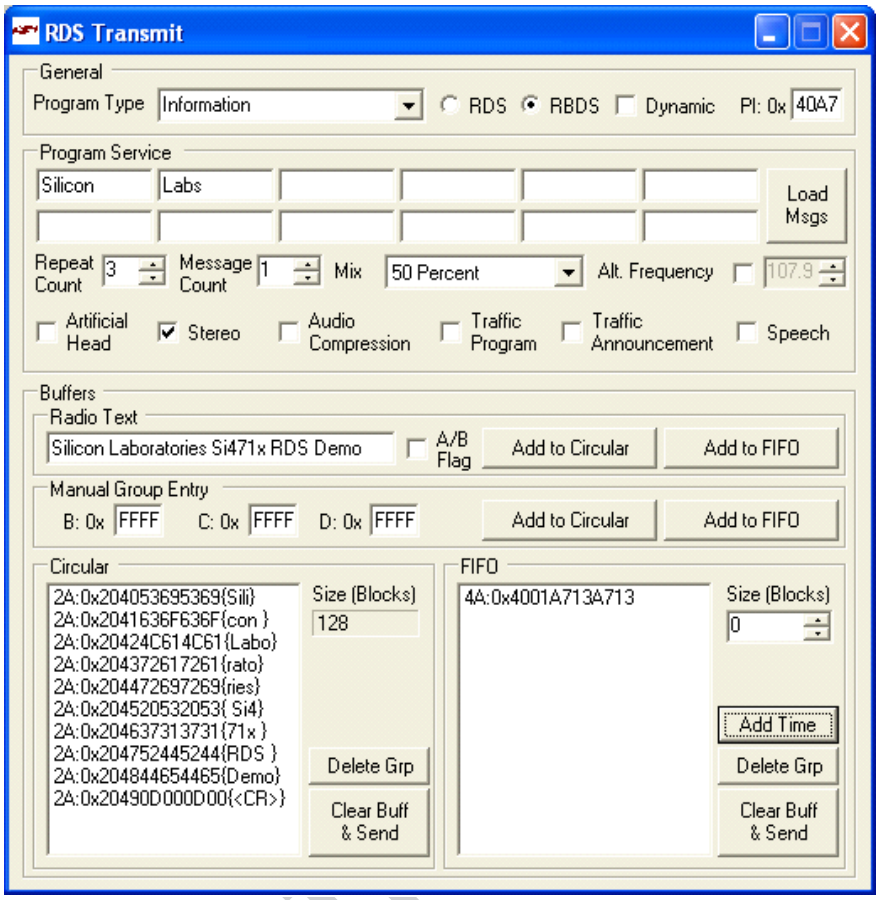

Figure 28. RDS Transmit Window

Table 7. RDS Window Explanations

Item	Explanation
General	
RDS / RBDS Selection	Select either RDS format (Europe) or RBDS format (US).
Program Type (PTY)	Select the available Program Type (PTY) from the pulldown menu.
PTY Dynamic	Select whether the PTY will be dynamic or static.
PI	Enter Program Identification (PI) code here.
Program Service	
Program Service Boxes	Enter up to 12 different Program Service (PS). Each PS consists of a maximum 8 characters.
Load Messages	Load the PS messages to the Si4711/13 chip.
Repeat Count	Enter how many time each PS will be repeated before sending the next PS.
Message Count	Enter how many messages of the loaded PS that will actually be transmitted.
Mix	Select the mix percentage between transmitting the Program Service or Buffers.
Alternate Frequency	Part of RDS Group Type 0 (PS): Enter Alternate Frequency if it is available.
Artificial Head	Part of RDS Group Type 0 (PS): Enter whether Artificial Head is On or Off.

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Table 7. RDS Window Explanations

Item	Explanation
Stereo	Part of RDS Group Type 0 (PS): Enter whether the transmitted audio is Stereo or Mono.
Audio Compression	Part of RDS Group Type 0 (PS): Enter whether the Audio Compression is On or Off.
Traffic Program	Part of RDS Group Type 0 (PS): Enter whether Traffic Program is available or not.
Traffic Announcement	Part of RDS Group Type 0 (PS): Enter whether Traffic Announcement is available or not.
Speech	Part of RDS Group Type 0 (PS): Enter between Speech or Music transmission.
Buffers	
Radio Text	Enter the RDS Group Type 2 Radio Text (RT) messages that will be uploaded to either the circular or FIFO buffer.
Radio Text: A/B Flag	Part of RDS Group Type 2 (RT): Enter whether the A/B Flag is set or not in entering the RT. This A/B Flag will tell the receiver to clear the display when the flag toggles from one state to the other.
Radio Text: Add to Circular	Add the RT messages that are typed into the circular buffers.
Radio Text: Add to FIFO	Add the RT messages that are typed into the FIFO buffers.
Manual Group Entry: B	Enter manual RDS entry block B. With this window you can practically transmit all RDS Group Type 0 through 15.
Manual Group Entry: C	Enter manual RDS entry block C. With this window you can practically transmit all RDS Group Type 0 through 15.
Manual Group Entry: D	Enter manual RDS entry block D. With this window you can practically transmit all RDS Group Type 0 through 15.
Manual Group Entry: Add to Circular	Add the RDS manual entry into the circular buffers.
Manual Group Entry: Add to FIFO	Add the RDS manual entry into the circular buffer.
Circular	Indicator showing the data that will be sent to the circular buffers.
Circular: Size (Blocks)	Indicator showing the size (in blocks) of the circular buffer. The total size of the buffer is 128 which is shared between the circular and FIFO buffers. To adjust the size, please change the size in the FIFO buffers.
Circular: Delete Group	Delete a group that is selected in the Circular Indicator window.
Circular: Clear Buffer & Send	Clear the data that is currently in the circular buffer and load it with the new one that is displayed in the circular indicator window.
FIFO	Indicator showing the data that will be sent to the FIFO buffers.
FIFO: Size (Blocks)	Indicator showing the size (in blocks) of the FIFO buffer. Adjusting the size of the FIFO, will also adjust the size of the circular buffer. The total of those two buffers are 128 blocks.
FIFO: Add Time	This will get the current time and format it into RDS Group Type 4 Clock & Time (CT), sent to the FIFO indicator window and have it ready to be loaded into the FIFO buffers.
FIFO: Delete Group	Delete a group that is selected in the FIFO Indicator window.
FIFO: Clear Buffer & Send	Clear the data that is currently in the FIFO buffer and load it with the new one that is displayed in the FIFO indicator window.

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There are 16 different group types in the RDS/RBDS standard, and for every group the following information is always transmitted:

1. Program Identification (PI)
2. Program Type (PTY)

The Si47xx GUI makes it easy to send data in 3 of the following group types:

1. Group Type 0: Program Service (PS)
2. Group Type 2: Radio Text (RT)
3. Group Type 4: Clock Time (CT)

It is possible to send data in the other group types, but the user has to manually enter the data in hexadecimal code.

Because of the complexity of the RDS/RBDS standard, the explanation of the RDS Transmit Data window is divided into three sections: Basic, Intermediate, and Advanced.

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6.8.1. Basic

The RDS Transmit Window is divided into three categories:

1. General
2. Program Service
3. Buffers

In the basic section, we will cover two out of the three categories, which are the General and Program Service. In the General category the user can set the PI and PTY data, while in the Program Service user will set the PS data (Group Type 0). The following diagram shows a step-by-step explanation of how to do it:

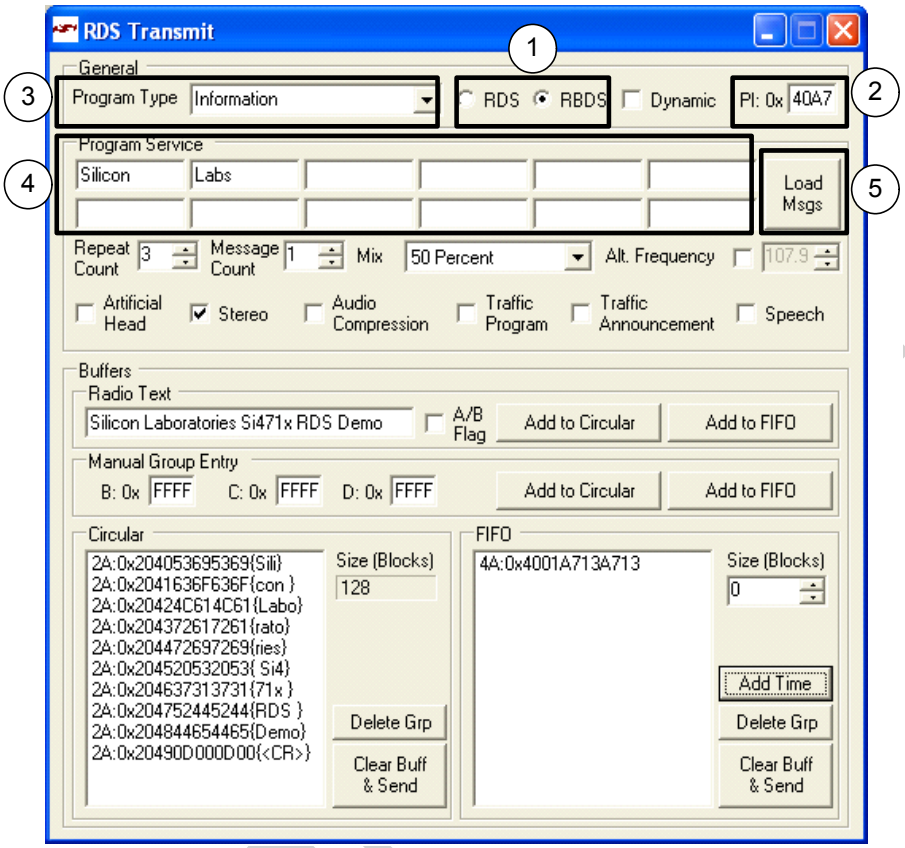

Figure 29. Basic RDS Sending Message Illustration

1. First select whether you want to transmit in RDS format (Europe) or RBDS format (US)
2. Type in the Program Identification in this field. Program Identification is a 16bit code assigned to individual station.
3. Select the Program Type in the pulldown menu here. There are a lot of different program types and some of the examples are: news, information, sports, talk, rock, etc.
4. Enter the Program Service (PS) in the boxes provided:
   a. You can enter a maximum of 12 different PS messages, in which each PS message can contain a maximum of 8 characters.
   b. Repeat Count: Enter how many times you want each PS message is transmitted before sending the next PS message.
   c. Message Count: Enter how many of the 12 PS message that you actually want to transmit.
   d. Mix: Put 100 percent here for now.
5. Click Send Message button here. Now the RDS will transmit the PS message along with the PI and PTY. You should see these data in your RDS receiver.

6.8.2. Intermediate

In the intermediate section, we will cover the buffers category of sending the RDS data with the Si4711/13, in particular we will send Group Type 2 (Radio Text) and Group Type 4 (Clock Time).

The following diagram shows a step-by-step procedure to send the buffers data in addition to the General and Program Service data covered in the basic section.

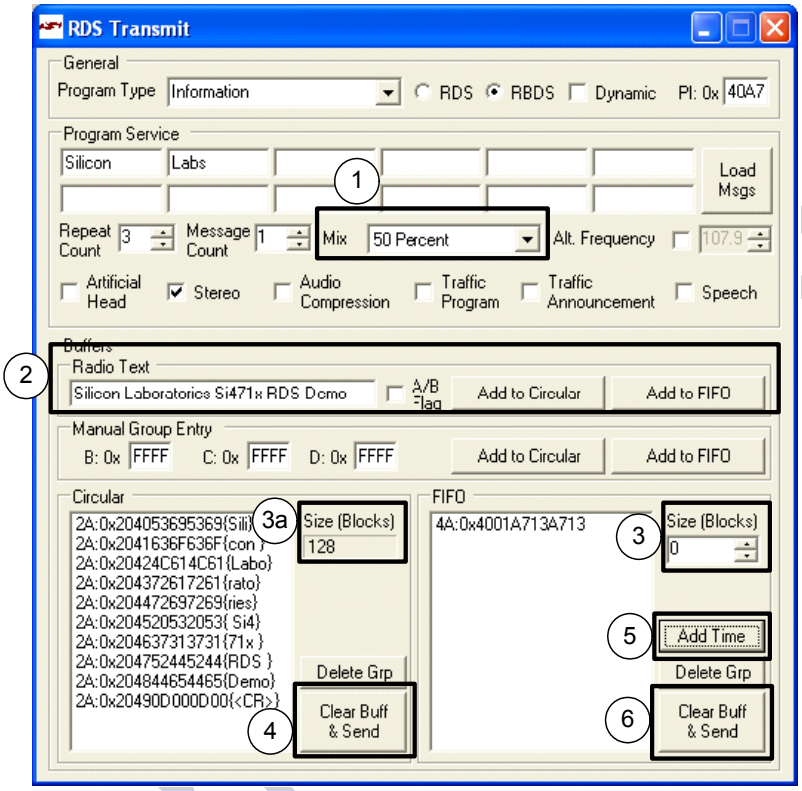

Figure 30. Intermediate RDS Sending Message Illustration

1. Select the Mix percentage that you want between transmitting the data in Program Service and the data in the Buffers. 100% means that you will always transmit the PS message regardless of what is contained in the Buffers, while 0% means that you will always transmit the data in the Buffers regardless of what is contained in the PS. If the buffers are empty though, the PS messages will be transmitted all the time regardless of the mix percentage.
2. Enter the Radio Text message that will be transmitted. After entering the RT message, click either the "Add to Circular" button or the "Add to FIFO" button. The RT message will be encoded according to the RDS Group Type 2 rule.
   a. Clicking "Add to Circular" button means that you upload the RT message into the Circular Buffer Indicator Window. Note that the message itself has not been uploaded into the Circular Buffer inside the Si4711/13 until the Clear Buff & Send is clicked.
   b. Clicking "Add to FIFO" means that you upload the RT message into the FIFO Buffer Indicator Window. Note that the message itself has not been uploaded into the FIFO Buffer inside the Si4711/13 until the Clear Buff & Send is clicked.
3. Enter the size of the FIFO that you want here. The Si4711/13 buffer has a total of 128 blocks, which is shared by the circular buffer and the FIFO. Therefore the circular buffer size (shown in 3a) will be the remainder of the 128 blocks minus the FIFO size.
4. Clicking this "Clear Buff & Send" button will upload the message from the Circular Buffer Indicator Window into the Circular Buffer inside the Si4711/13. Circular buffer holds the message that will be transmitted over and over again. Note that the messages in the circular buffer will be transmitted only if the PS Mix value is set to anything other than 100%.
5. Clicking the "Add Time" button here will automatically upload the current time into the FIFO. The CT time data is uploaded into the Si4711 according the RDS Group Type 4 rule.
6. Clicking the "Clear Buff & Send" button will upload the message from the FIFO Buffer Indicator Window into the FIFO Buffer inside the Si4711/13. FIFO buffer holds the message that will be transmitted only once. A good example of using FIFO buffer is when you want to send the time data. Time is something that occurs only once, so it will not be beneficial to upload time to the circular buffer and get transmitted continuously. We will cover how to send time in step #5. Note that the messages in the FIFO buffer will be transmitted only if the PS Mix value is set to anything other than 100%.

6.8.3. Advanced

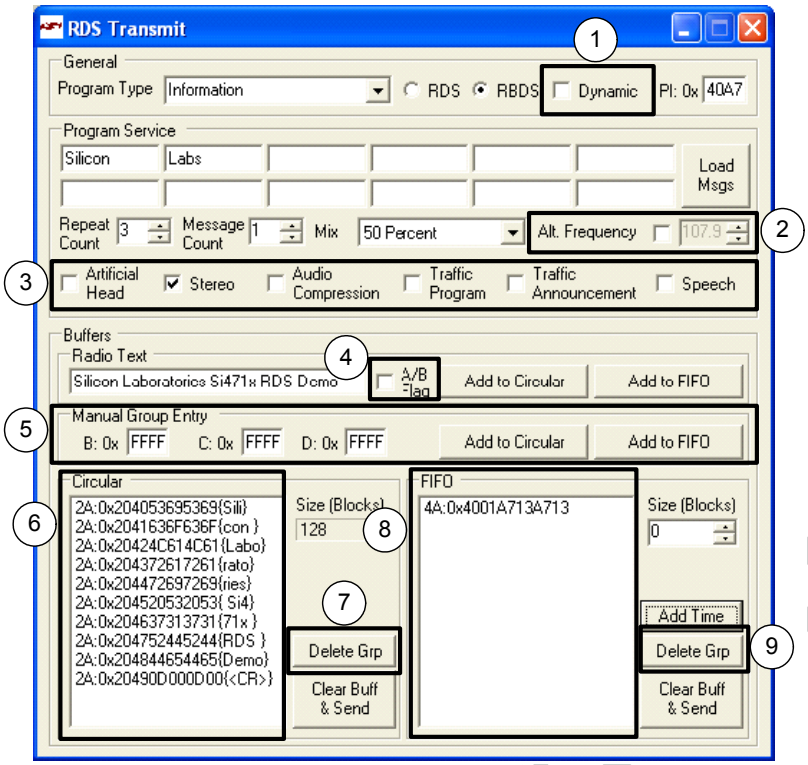

Figure 31. Advanced RDS Sending Message Illustration

1. Dynamic: This tells whether the PTY code is static or dynamic.
2. Alternate Frequency: This provides the ability to inform the receiver of a single alternate frequency. This field is transmitted along with the Group Type 0 (PS).
3. Miscellaneous bits in Group Type 0 (PS):
   a. Artificial Head: 0 = Not Artificial Head, 1 = Artificial Head
   b. Stereo: 0 = Mono, 1 = Stereo
   c. Audio Compressor: 0 = Not compressed, 1 = Compressed
   d. Traffic Program (TP): 0 = No TP, 1 = TP
   e. Traffic Announcement (TA): 0 = No TA, 1 = TA
   f. Speech: 0 = Speech, 1= Music
4. A/B Flag: This is an important flag in the RDS Group Type 2 (RT). Checking this box when a Radio Text is uploaded means that the RT is uploaded with the flag set. Unchecking this box when an RT is uploaded means that the flag is not set. This flag tells the receiver that when the flag toggles from set to reset or vice versa, the receiver will clear the display before showing the next RT.
5. Manual Group Entry: This is the box if used needs to upload the RDS data manually. User can use this box for uploading message from Group Type that the Si47xx GUI does not have encoding support, in which users has to encode the message into hexadecimal code by themselves.
6. Circular Buffer Indicator: This displays the message that gets uploaded into the Circular Buffer in hexadecimal code. This can be useful to see how the Group Type 0 (PS), Type 2 (RT), and Type 4 (CT) is encoded into RDS data.
7. Delete Circular Buffer Group: This deletes a group that is selected in the Circular Buffer Indicator.
8. FIFO Buffer Indicator: This displays the message that gets uploaded into the FIFO buffer in hexadecimal code.
9. Delete FIFO Buffer Group: This deletes a group that is selected in the FIFO Buffer Indicator.

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7. Schematics

7.1. Si471x Baseboard

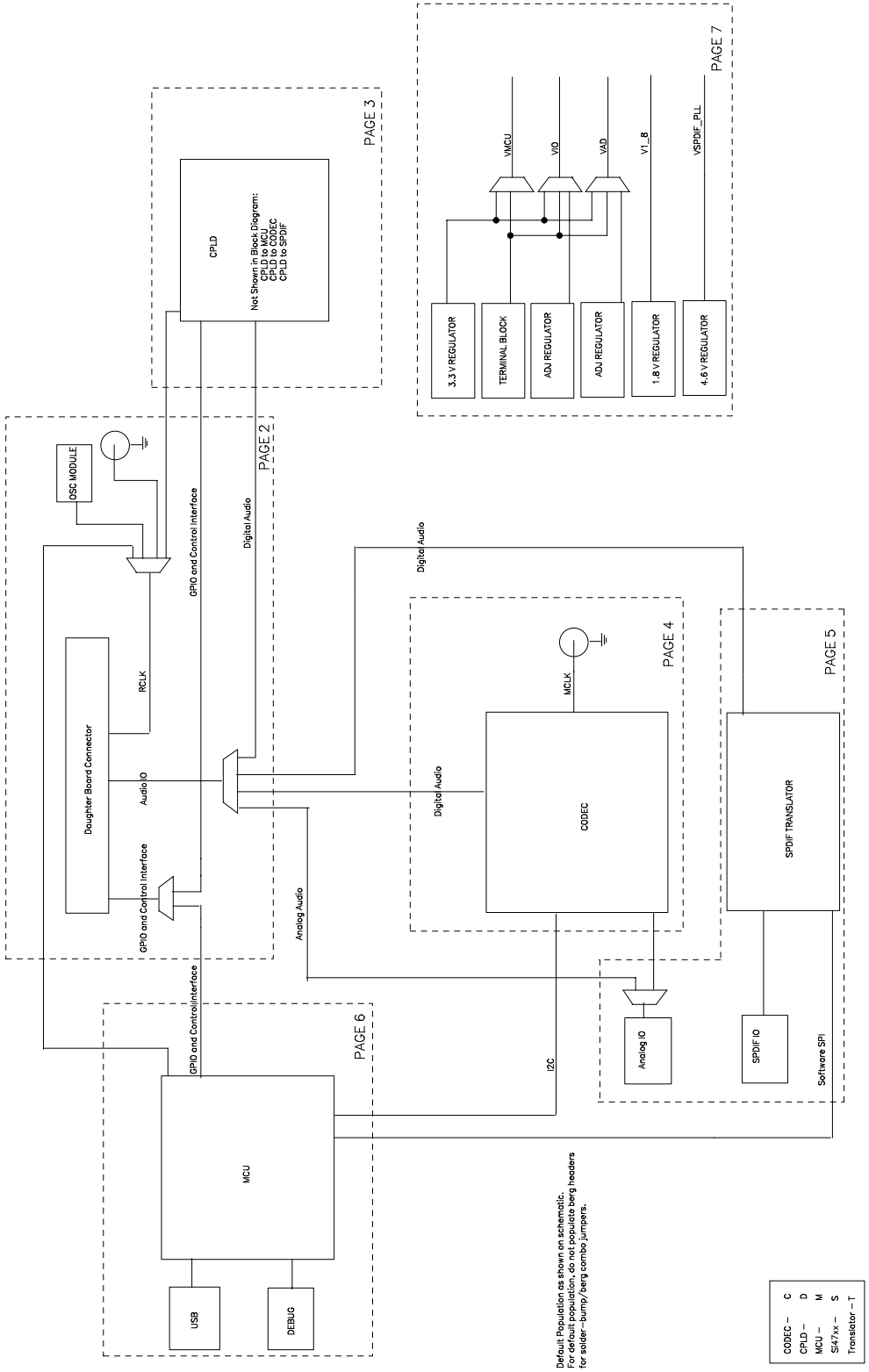

Figure 32. Si471x Baseboard - Block Diagram

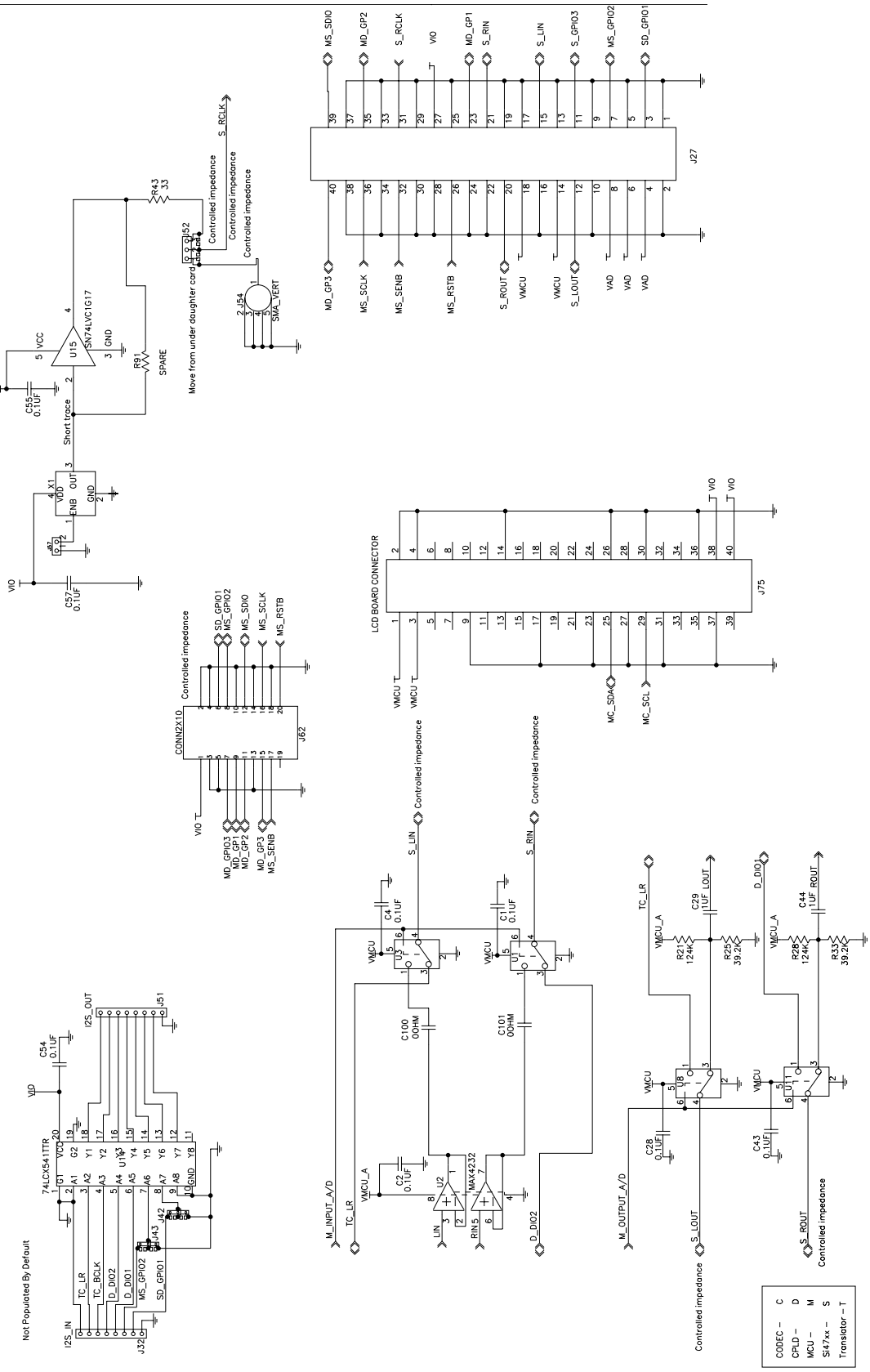

Figure 33. Si471x Baseboard - Daughter Card Interface

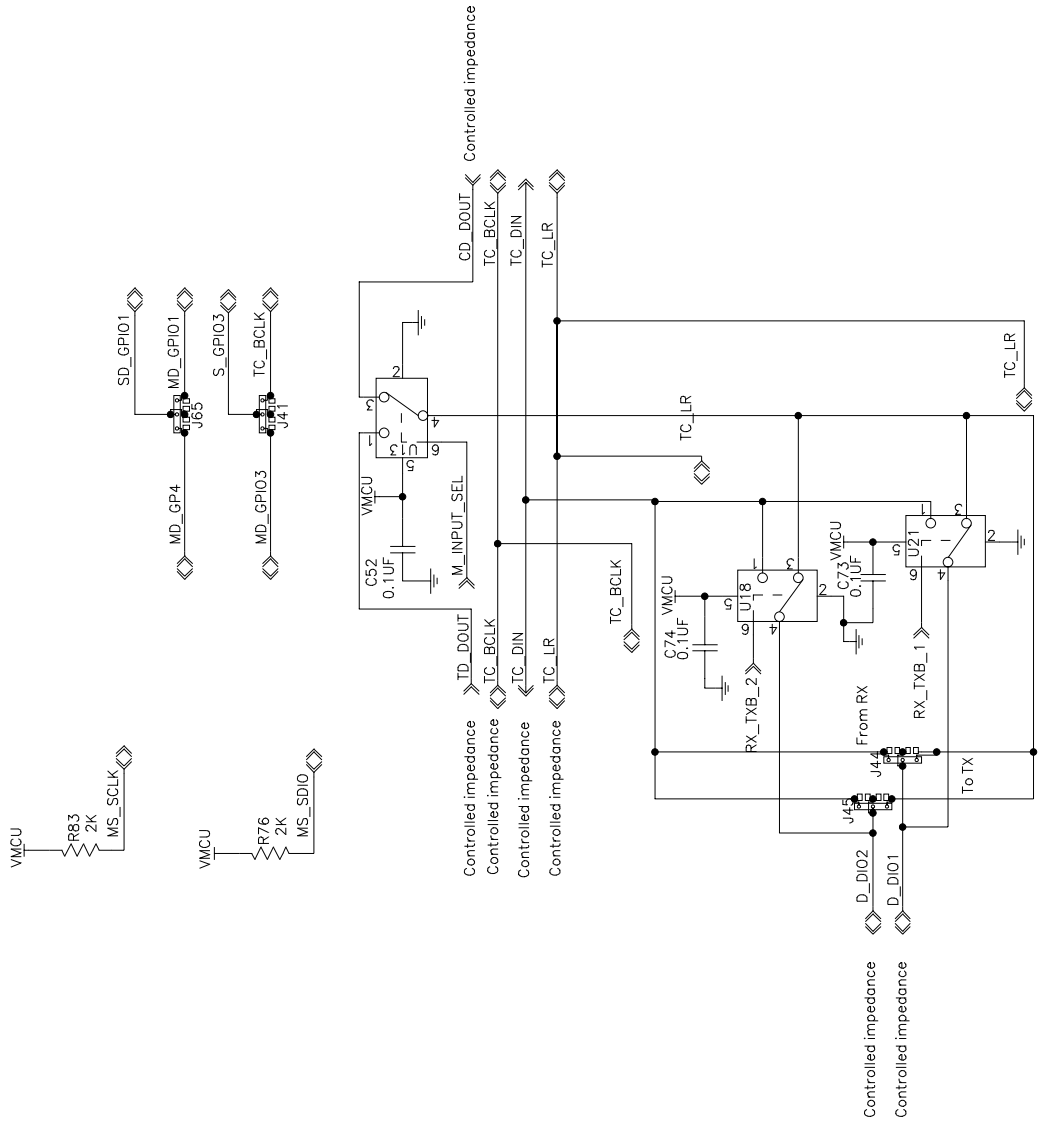

Figure 34. Si471x Baseboard - Signal Multiplexers

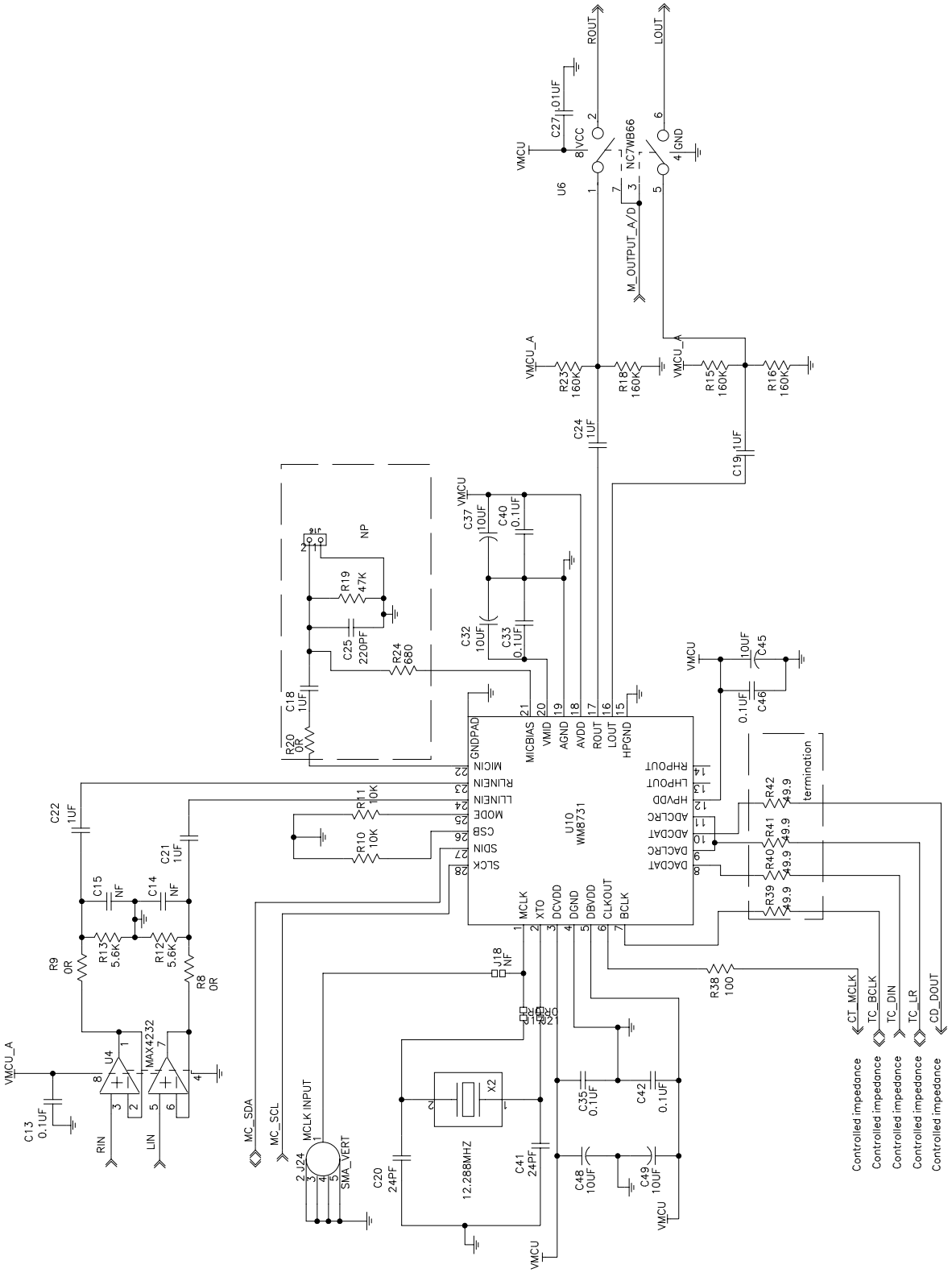

Figure 35. Si471x Baseboard - CODEC

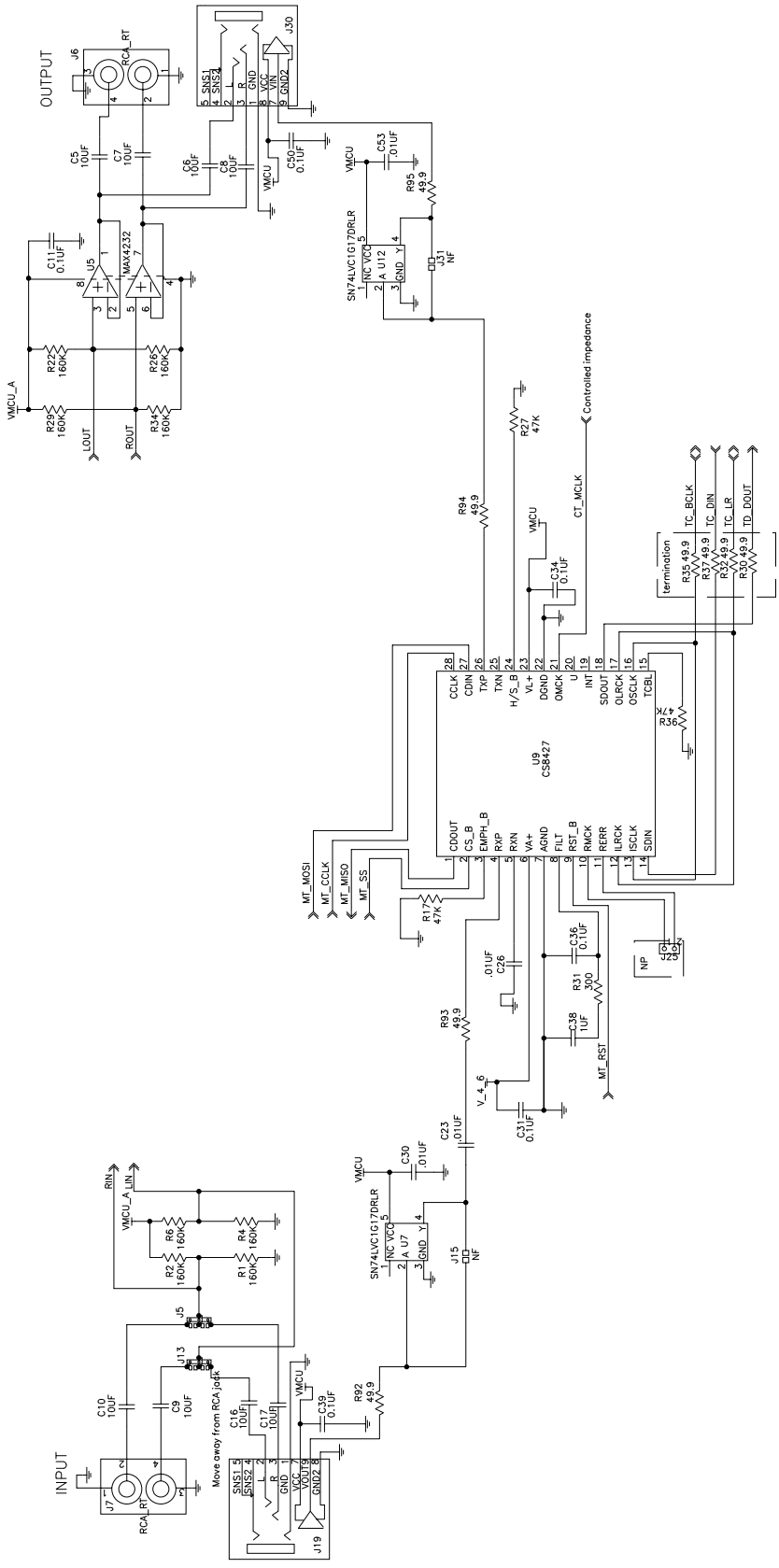

Figure 36. Si471x Baseboard - Audio Input and SPDIF Translator

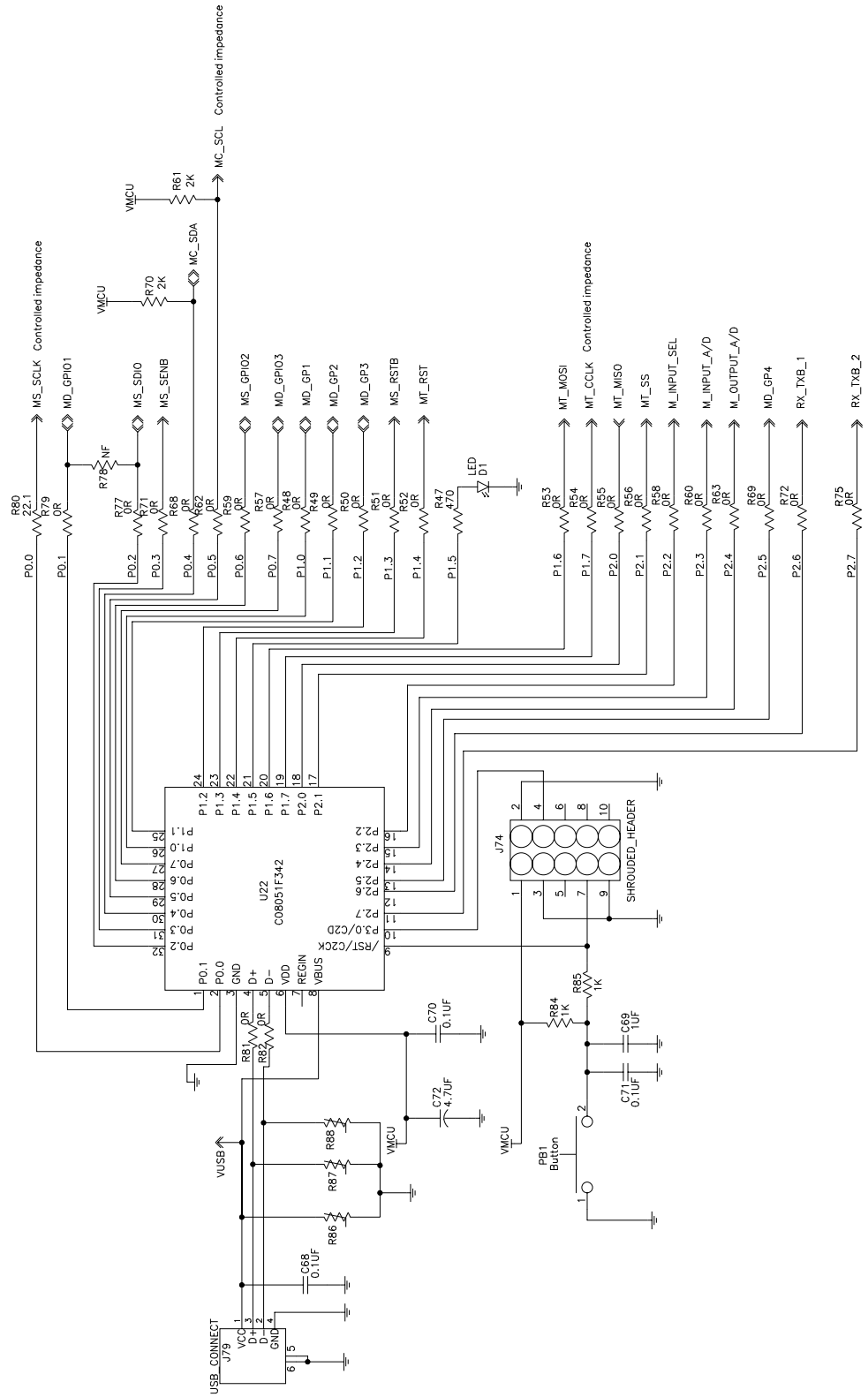

Figure 37. Si471x Baseboard - MCU

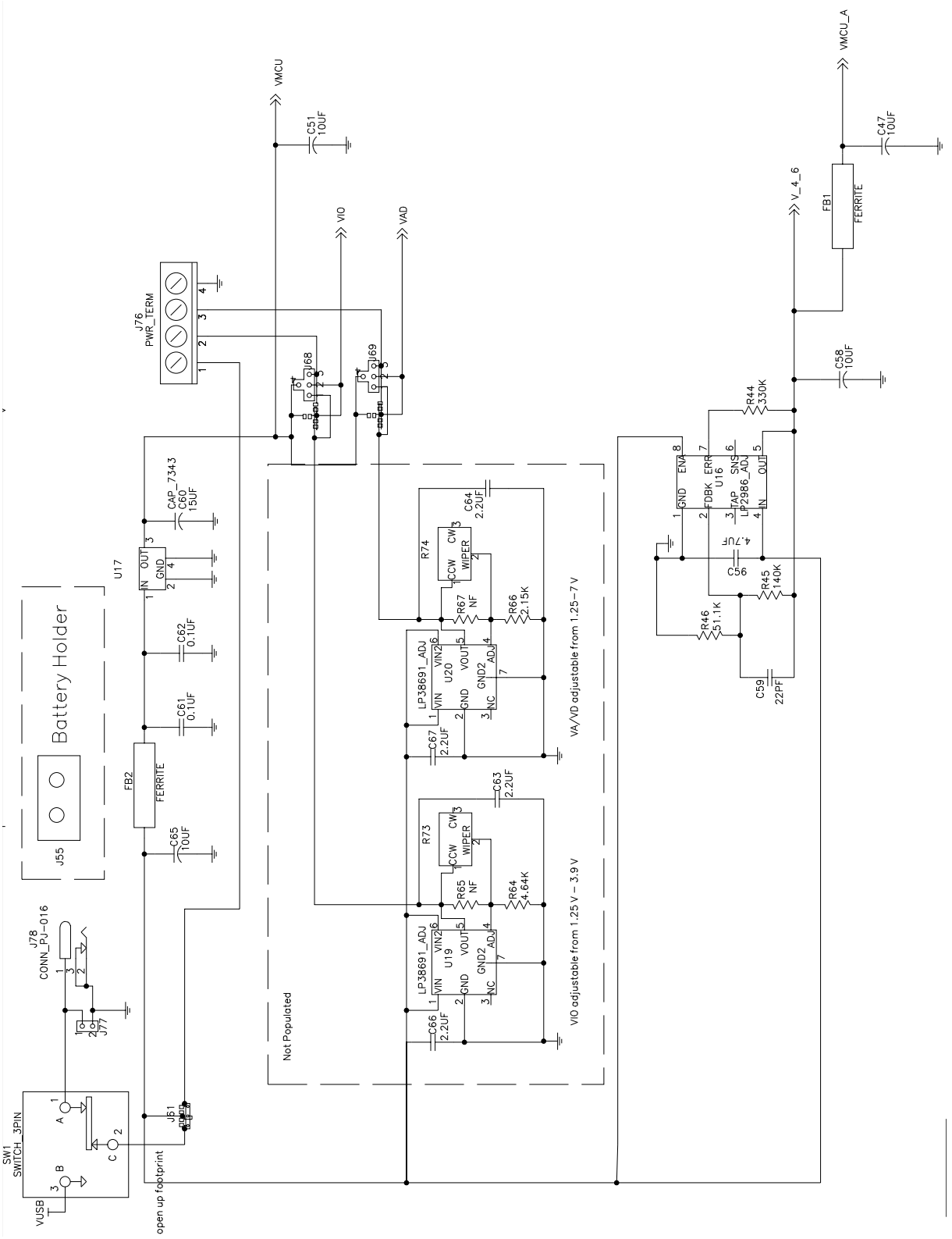

Figure 38. Si471x Baseboard - Power Supply

7.2. Si471x Daughter Card

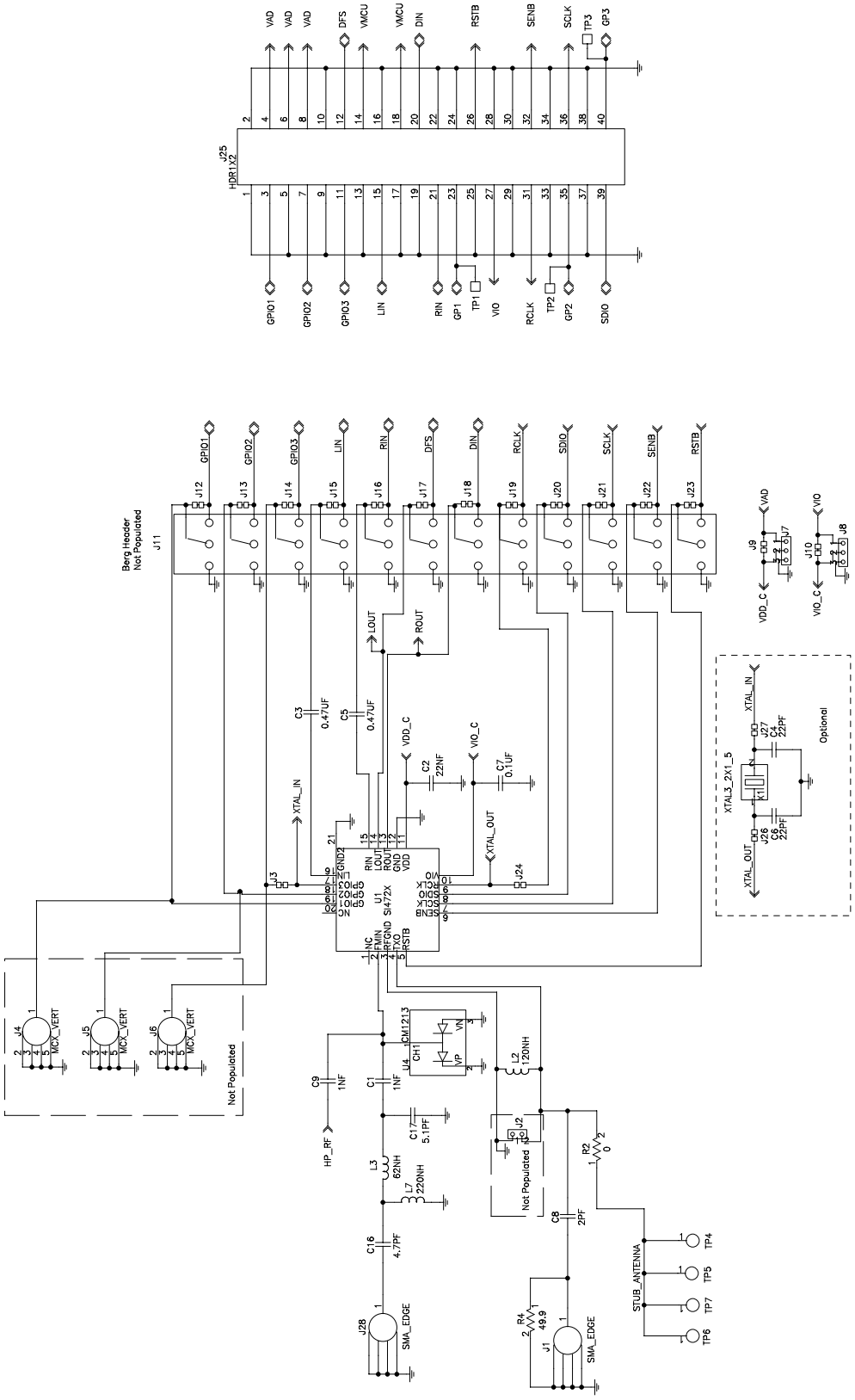

Figure 39. Si471x Daughter Card

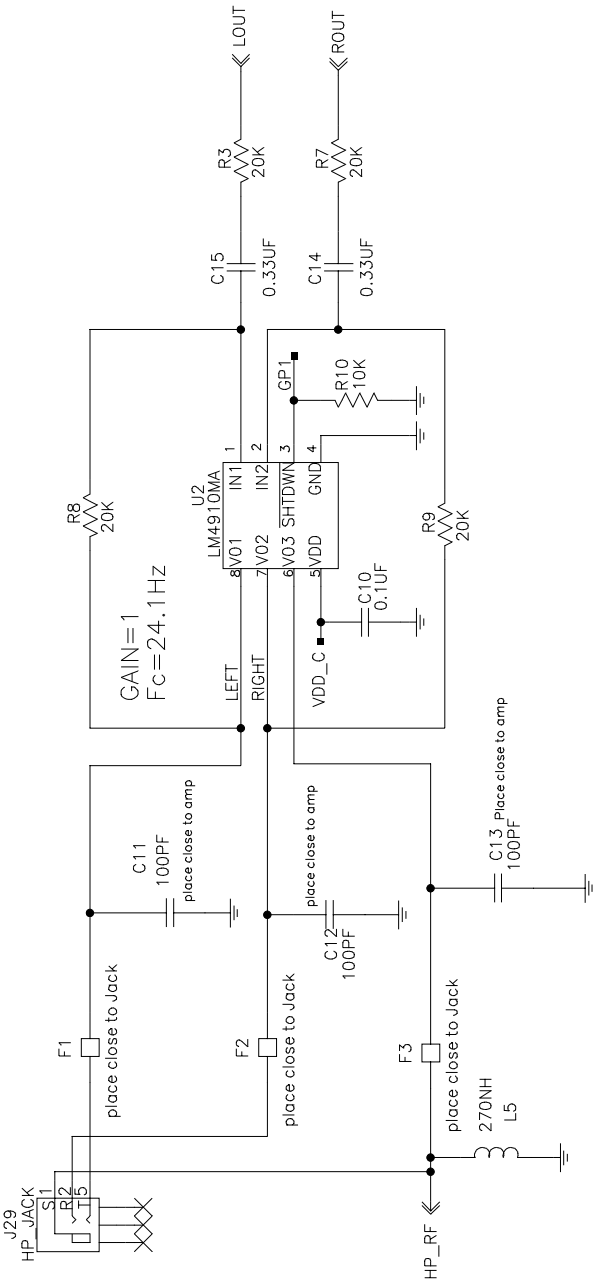

Figure 40. Daughter Card Headphone Schematic (applies only to Si472x)

8. Layout

8.1. Si471x Baseboard

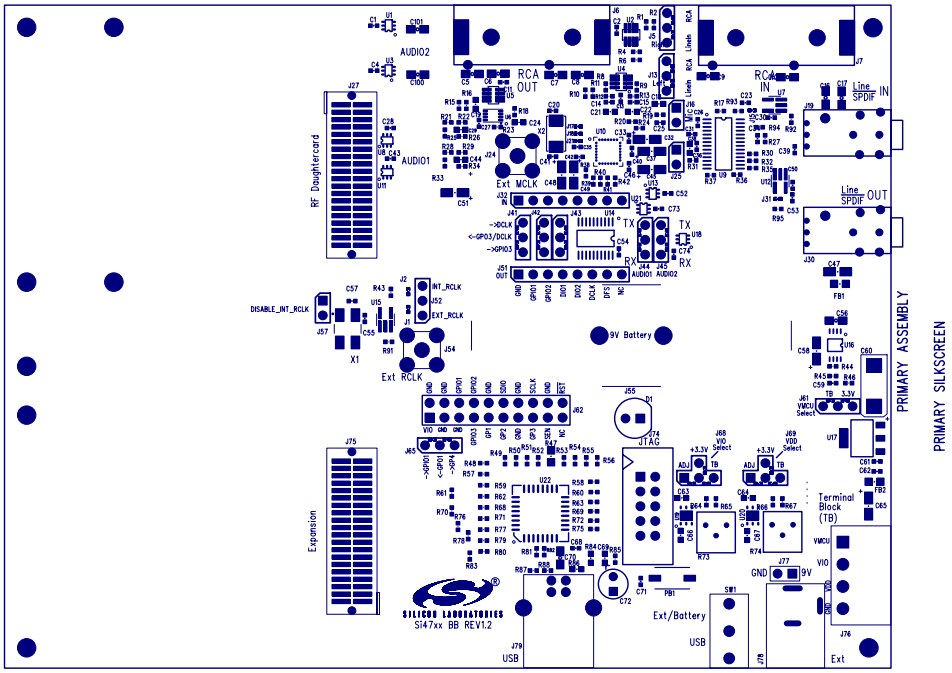

Figure 41. Si471x Baseboard - Primary Assembly Silkscreen

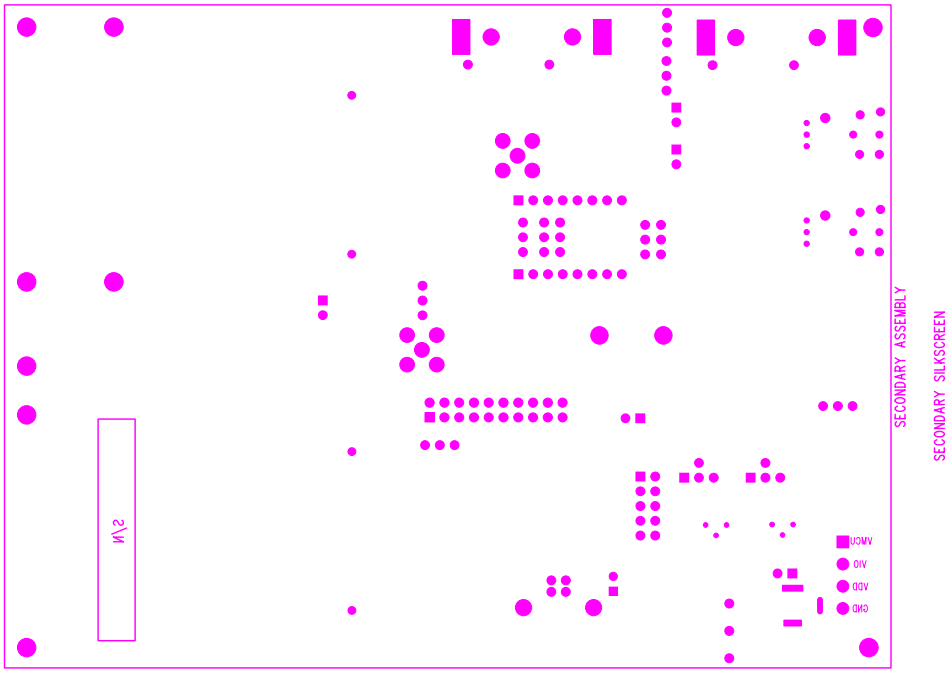

Figure 42. Si471x Baseboard - Secondary Assembly Silkscreen

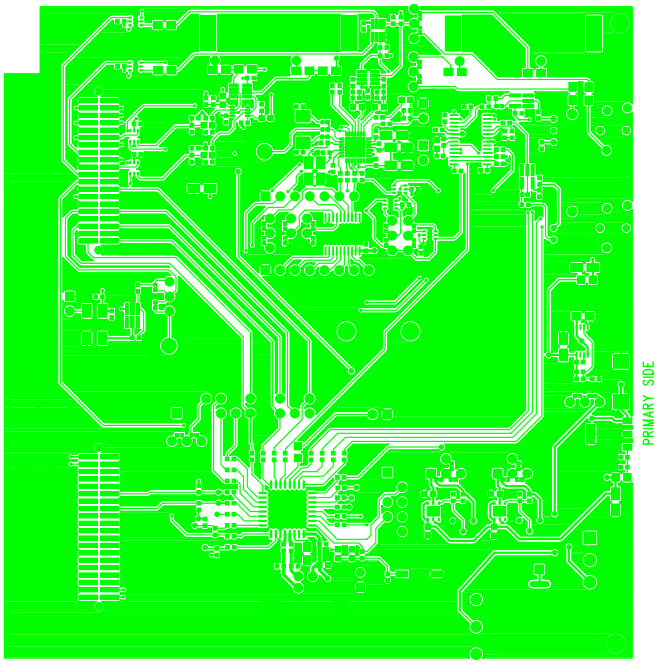

Figure 43. Si471x Baseboard - Primary Side

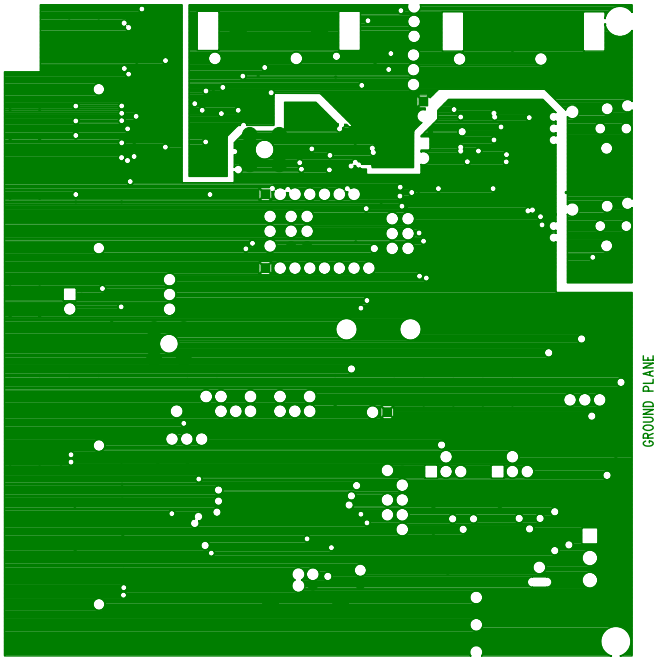

Figure 44. Si471x Baseboard - Ground Plane

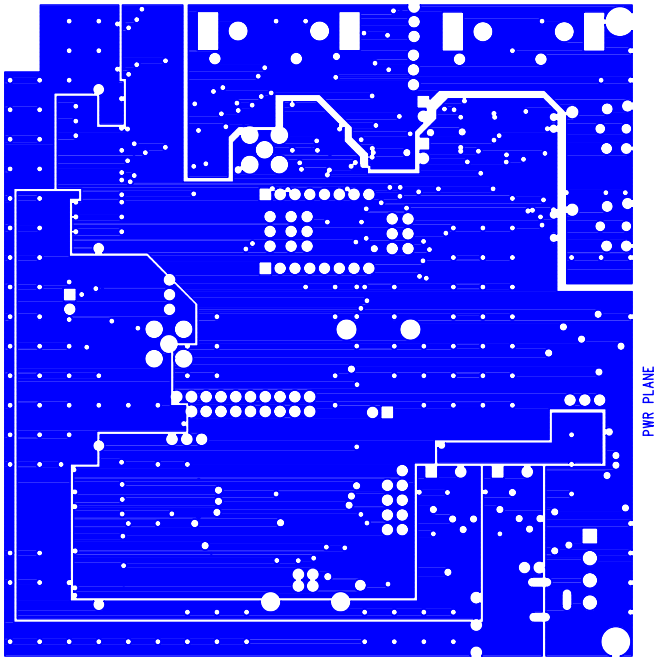

Figure 45. Si471x Baseboard - Power Plane

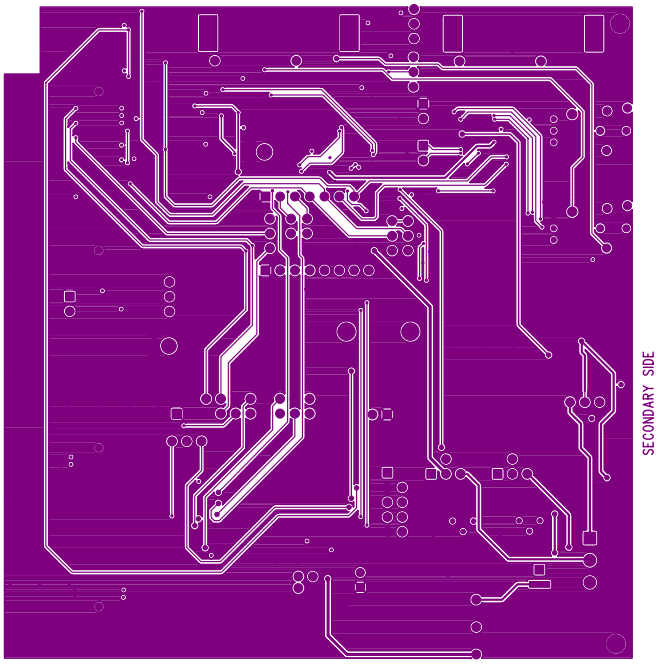

Figure 46. Si471x Baseboard - Secondary Side

8.2. Si471x Daughter Card

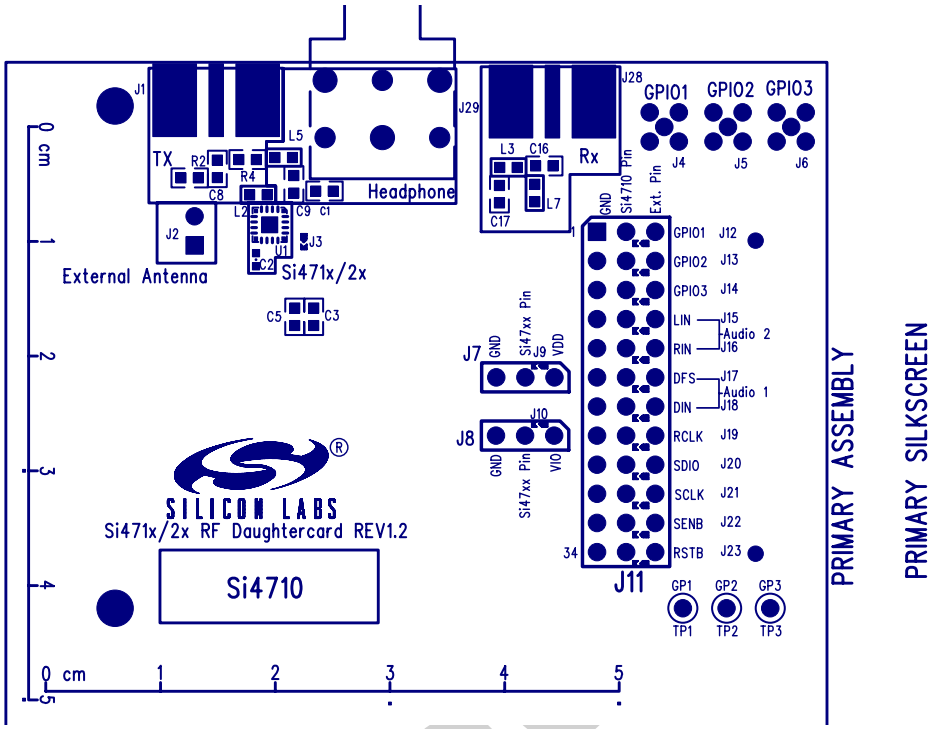

Figure 47. Si471x Daughter Card - Primary Assembly Silkscreen

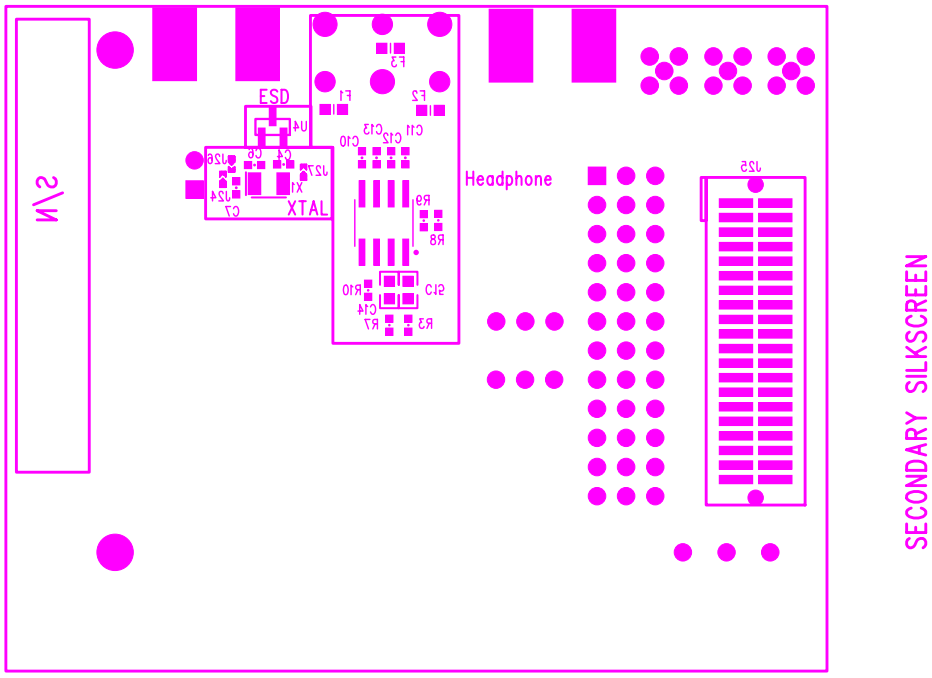

Figure 48. Si471x Baseboard - Secondary Assembly Silkscreen

Figure 49. Si471x Baseboard - Primary Side

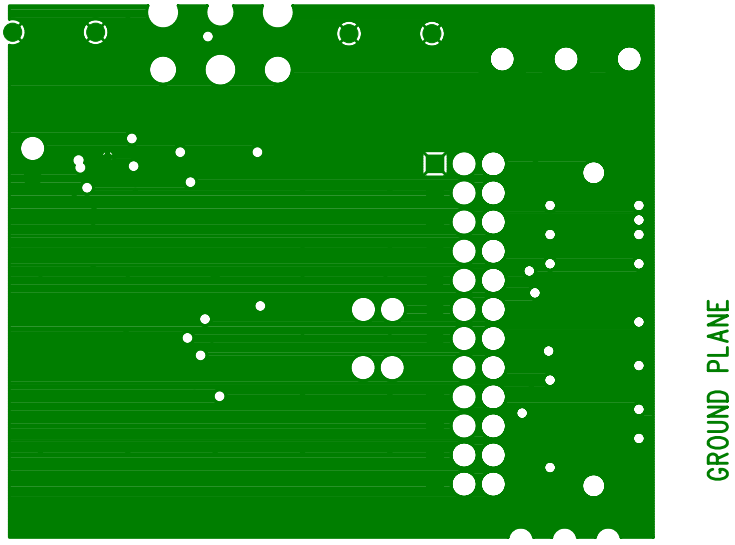

Figure 50. Si471x Baseboard - Ground Plane

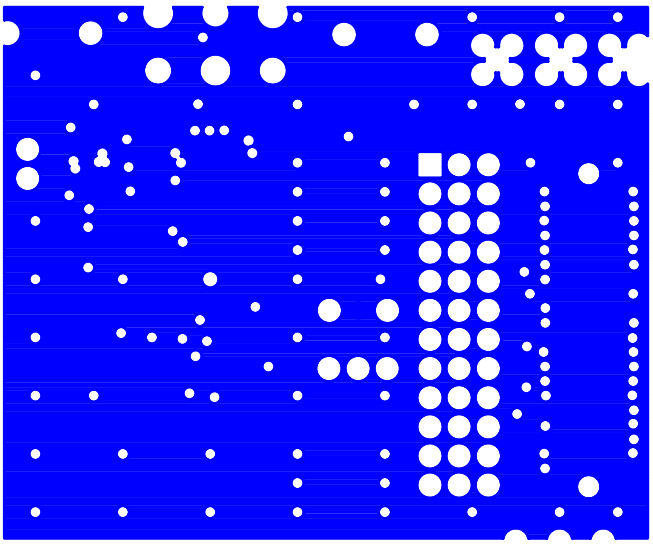

Figure 51. Si471x Baseboard - Power Plane

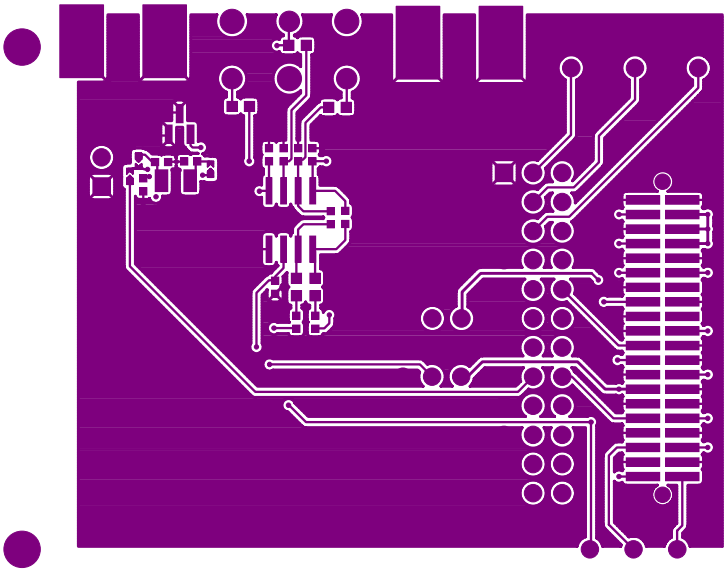

Figure 52. Si471x Baseboard - Secondary Side

9. Bill of Materials

Table 8. Si47xx Baseboard Rev1.3 - Bill of Materials

Item	Qty	REFDES	Description	Value	MFG/Vendor	MFG/Vendor_PN
1	1	J78	2.1 mm power plug		CUI	CONN_PJ-01
2	27	C1,C2,C4,C11,C13,C28,C31,C33,C34, C35,C36,C39,C40,C42,C43,C46,C50, C52,C54,C55,C57,C61,C62,C68,C71, C73,C74	CAP,SM,0402,0.1UF,10%	0.1 UF	VENKEL	C0402X7R160-104KNE
3	1	C72	RADIAL CAP	4.7 UF	Kemet	T350B475K016AS
4	1	C70	CAP,SM,0805	0.1 UF		
5	1	C60	CAP,SM,7343,15UF,10%	15 UF	VISHAY	293D156X9020D2T
6	9	C18,C19,C21,C22,C24,C29,C38,C44, C69	CAP,SM,0603,1UF,X7R	1 UF	VENKEL	C0603X7R100-105KNE
7	2	C20,C41	CAP,SM,0402	24 pf	MURATA	GRM1555C1H240JZ01D
8	5	C23,C26,C27,C30,C53	CAP,SM,0402,.01UF,10%,25V	0.01 uF	Kemet	C0402C103K3RACTU
9	1	C59	CAP,SM,0402,22PF,10%	22 Pf	PANASONIC-ECG	ECJ-0EC1H220J
10	8	C32,C37,C45,C47,C48,C49,C51,C65	CAP,SM,3216,16V	10 UF	VISHAY	293D106X9016A2
11	8	C5,C6,C7,C8,C9,C10,C16,C17	CAP,SM,0805	10 UF	MURATA	
12	1	C25	CAP,SM,0402,220PF,5%	220 PF	PANASONIC - ECG	ECJ-0EC1H221J
13	1	C58	CAP,SM,3216,10V,10%,6.8UF	6.8 UF	EPCOS INC	B45196H2685K109
14	1	C56	CAP,SM,0805,25V,10%,4.7UF	4.7 UF	MURATA	GRM21BR61E475KA12 L
15	1	D1	LED,T-1 3/4.RED DIFFUSED		LITEON	LTL-10223W
16	2	FB1,FB2	FERRITE BEAD,SM		STEWARD	MI0805K400R-00
17	2	C100, C101	RES,SM,0805	0 ohm	Venkel	
18	15	J5,J13,J41,J44,J45,J61,J65	CONN,TH,1X3,HDR		SAMTEC	TSW-103-07-G-S
19	1	J62	CONN,TH,2X10,HDR		SAMTEC	TSW-110-07-G-D
20	1	J76	PCB TERMINAL BLOCK, 4 POSI-TION		MOUSER ELECTRONICS	651-1803293
21	2	J27,J75	CONN,TH,TFM,HDR,2X20,0.05X0 .05IN PITCH		SAMTEC	TFM-120-02-S-D-A
22	2	J24,J54	SMA_VERTICAL		Digikey	ARFX1231-ND
23	2	J32,J51	CONN,TH,1X8,HDR		SAMTEC	TSW-108-07-G-S
24	4	J68, J69	CONN,TH,1X3,HDR\ CONN,TH,1X1,HDR		SAMTEC	TSW-103-07-G-S\ TSW-101-07-G-S
25	2	J6,J7	CONN,RCA,RIGHT ANGLE		CUI	RCJ-2123
26	1	J30	MINIJACK,3.3V,8MBPS		SHARP	GP1FD310TP
27	1	J19	MINIJACK,RCVR,3.3V,8MBPS		SHARP	GP1FD210RP
28	1	J74	HEADER,SHROUDED,5X2		3M	2510-6002UB
29	1	J79	CONN,TH,USB,RCPT,TYPE B		67068-0000	MOLEX/WALDOM ELECTRO
30	1	PB1	BUTTON,SM, LIGHT-TOUCH,160GF,6X3.5MM		PANASONIC - ECG	EVQ-PPBA25
31	28	R8,R9,R20,R48,R49,R50,R51,R52, R53,R54,R55,R56,R57,R58,R59,R60, R62,R63,R68,R69,R71,R72,R75,R77, R79,R81,R82,R91	RES,SM,0402	0R	VENKEL	CR0402-16W-000T
32	1	R80	RES,SM,0402	22.1	VENKEL	CR0402-16W-22R1FT
33	2	R10,R11	RES,SM,0402	10K	KOA SPEER	RK73H1ELTP1002F
34	2	R12,R13	RES,SM,0402	5.6K	KOA SPEER	RK73H1ELTP5601F
35	1	R43	RES,SM,0402	33	VENKEL	CR0402-16W-330GT
36	4	R17,R27,R36,R19	RES,SM,0402	47K	YAGEO CORPORATION	RC0402FR-0747KL
37	1	R31	RES,SM,0402,300,1%,1/16W	301	YAGEO CORPORATION	9C04021A3010FLHF3
38	1	R38	RES,SM,0402,100,1%,1/16W	100	YAGEO CORPORATION	RC0402FR-07100RL

Table 8. Si47xx Baseboard Rev1.3 - Bill of Materials (Continued)

Item	Qty	REFDES	Description	Value	MFG/Vendor	MFG/Vendor_PN
39	12	R1,R2,R4,R6,R15,R16,R18,R22,R23, R26,R29,R34	RES,SM,0402,160K,5%	160K	VENKEL	CR0402-16W-164JT
40	1	R85	RES,SM,0402	1K	VENKEL	CR0402-16W-102J
41	4	R61,R70,R76,R83	RES,SM,0402	2K	VENKEL	CR0402-16W-202J
42	1	R47	RES,SM,0805	470	VENKEL	CR0805-8W-471J
43	1	R46	RES,SM,0402,1%	51.1K	ROHM	MCR01MZPF5112
44	1	R45	RES,SM,0402,1%	140K	PANASONIC-ECG	ERJ-2RKF1403X
45	1	R44	RES,SM,0402	330K	ROHM	MCR01MZPJ334
46	2	R21,R28	RES,SM,0402	124K	ROHM	MCR01MZPF1243
47	2	R25,R33	RES,SM,0402	39.2K	ROHM	MCR01MZPF3922
48	1	R84	RES,SM,0603	1K	VENKEL	CR0603-10W-1001FT
49	1	R86	VARISTOR,SM,O603		LITTLEFUSE INC	V5.5MLA0603H
50	2	R87,R88	VARISTOR,SM,O402		LITTLEFUSE INC	V0402MHS03
51	1	R24	RES,SM,0402,680,1%,1/16W	681	ROHM	MCR01MZPF6810
52	1	SW1	SWITCH_3PIN		e-switch	eg2472
53	7	U1,U3,U8,U11,U13,U18,U21	SPDT_SWITCH,SC70-6		FAIRCHILD	NC7SB3157P6X
54	1	U17	VOLTAGE_REG,3_3 V,500MA,SOT223		NATIONAL SEMICONDUCT	LM2937IMP-3.3
55	1	U14	OCTAL_BUFFER,TSSOP-20		ST	74LCX541TTR
56	3	U7,U12,	IC,SINGLE_SCHMITT_TRIGGER _BUFFER		TEXAS_ INSTRUMENTS	SN74LVC1G17DBVR
57	3	U2,U4,U5	IC,SM,OPAMP,SOT23-8		MAXIM	MAX4232AKA-T
58	1	U16	VOLTAGE_REG,ADJV V,200MA		NATIONAL SEMICONDUCT	LP2986-5.0
59	1	U10	IC,SM,WM8731,WOLFSON,QFN-28		WOLFSON	WM8731
60	1	U6	IC,SM,UHS DUAL SPST,8 LEAD US8		FAIRCHILD SEMICONDUC	FSA266K8X
61	1	U22	IC,SM,C8051F342,MCU,LQFP-32,9X9MM		SILICON LABORATORIES	C8051F342GQ
62	1	U9	IC,SM,CS8427-DS,SPDIF_TRANSLATOR,28-TSSO		CIRRUS	CS8427-CZ
63	1	X1	32_768KHZ,OSCILLATOR,SM		ECS_INC	ECS-327SMO
64	1	X2	XTAL,12.288MHZ,18PF		CITIZEN AMERICA CORP	CS10-12.288MABJ-UT
65	1	R30,R32,R35,R37,R39,R40,R41,R42, R92,R93,R94,R95	Res,sm,0402	49.9	Venkel	CR0402-16W-49R9FT
66	1	J76	4P Plug 180Deg terminal block		MOUSER ELECTRONICS	651-1803594
67	2		Screw Pan 440x3/4		MOUSER ELECTRONICS	561-P440.75
68	2		Spacer nyln rnd 4x.25		MOUSER ELECTRONICS	561-K4.25
69	3		Screw Pan 440x3/8		MOUSER ELECTRONICS	561-P440.375
70	5		1/4 Tapped spacer		MOUSER ELECTRONICS	561-TSP3
71	2		Steel nut, Size 2-56 Width 0.187'		Newark	18M5986
72	2		Steel Screw Head Diameter 0.162', Length 0.25', Size 2-56		Newark	18M6002
73	4		Nylon Washer, Diameter 0.187', Size #2		Newark	94F9852
74	1		Battery Holder 9 V		MOUSER ELECTRONICS	1BH080
75	1		"I" 6" 26AWG W/SKT 9 V Snap		MOUSER ELECTRONICS	121-0626/M-GR

Table 9. Si471x-EVB Daughter Card Rev1.2 - Bill of Materials

Item	Qty	REFDES	Description	Value	MFG/Vendor	MFG/Vendor_PN
1	2	C4,C6	CAP,SM,0402,X7R	22 PF	MURATA	GRM185R71E220KA61D
2	1	C2	CAP,SM,0402,X7R	22 NF	MURATA	GRM185R71E223KA61D
3	1	C7	CAP,SM,0402,X7R	0.1 UF	MURATA	GRM185R71C104KA88D
4	1	C10	CAP,SM,0402,X7R	0.1 UF	MURATA	GRM185R71C104KA88D
5	2	C3,C5	CAP,SM,0603,X7R	0.47 UF	VENKEL	C0603X7R160-474KNE
6	1	C1	CAP,SM,0603,X7R	NP	VENKEL	
7	1	C9	CAP,SM,0603,X7R	NP	VENKEL	
8	3	C11,C12,C13	CAP,SM,0402,X7R	NP	MURATA	GRM1555C1H101JZ01D
9	2	C14,C15	CAP,SM,0603,X7R	NP	VENKEL	C0603X7R160-334KNE
10	1	C17	CAP,SM,0603,X7R	NP		
11	1	J1	SMA,EDGE-MOUNT, GOLD PLATED		YAZAKI	RA2EJ2-6G
12	1	J28	SMA,EDGE-MOUNT, GOLD PLATED	NP	YAZAKI	RA2EJ2-6G
13	1	J25	CONN, SM, 2X20, SFM		SAMTEC	SFM-120-02-S-D-A
14	3	J4,J5,J6	CONN, THRU--HOLE, MCX JACK, .100 LAYOUT	MCX_VERT	DIGI-KEY	J611-ND
15	1	J11	HEADER, 3X12	NP	SAMTEC	TSW-112-07-G-T
16	16	J3,J9,J10,J12,J13,J14,J15,J16, J17,J18,J19,J20,J21,J22,J23,J24	SOLDER BUMP JUMPER, RES, SM, 0402			
17	2	J7,J8	CONN, TH, 1X3, HDR	NP	SAMTEC	TSW-103-07-G-S
18	1	J2	CONN, TH, 1X2, HDR	NP	SAMTEC	TSW-102-07-G-S
19	1	J29	CONN,AUDIO JACK,3.5MM,STEREO	NP	DIGIKEY	CP-3543N-ND
20	3	F1,F2,F3	Ferrite Bead,SM,0603	NP	MURATA	BLM18BD252SN1D
21	1	L2	IN, SM, 0603	120 nH	MURATA	lqw18anr12j00d
22	1	L5	IN, SM, 0603	NP	MURATA	LQW18ANR27J00D
23	1	L7	IN, SM, 0603	NP		
24	1	R2,	RES, SM, 0603	0R	VENKEL	CR0603-16W-000T
25	2	C16,L3	RES, SM, 0603	NP	VENKEL	CR0603-16W-000T
26	1	C8	RES,SM,0603	2 pF	AVX	06035J2R0ABTTR
27	1	R4	RES, SM, 0603	49.9 R	VENKEL	CR0603-16W-000T
28	1	R10	RES, SM, 0402	NP	VENKEL	CR0603-16W-103JT
29	4	R3,R7,R8,R9	RES,SM,0603	NP	VENKEL	CR0603-16W-203JB
30	1	U1	IC, SM, SI4710,MLP20 3X3		SILAB	SI4710
31	1	U2	IC,SM,HEADPHONE AMP	NP	NATIONAL SEMICONDUCTOR	LM4910MA
	1	U4	IC,SM,ESD PROTECTION DIODE,SOT23-3	NP	CALIFORNIA MICRO DEVICES	CM1213-01ST
32	1	X1	XTAL, SM, 32.768		Epson	FC-135
33	1	A1	4710 RF Daughter Card PCB			

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DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Updated Section “4. Recommended Hardware Setup” to include digital input support.
- Updated Section “5. Getting Started - Software Installation (Firmware 1.B)” to include digital input support.
- Updated Section “6. Development Using Si471x GUI (Firmware 1.B)” to include digital input properties.

Revision 0.3 to Revision 0.4

- Added RDS feature.
- Added Limiter feature.
- Added Overmodulation Indicator.
- Updated all schematics and layout images.
- Added Table 8, “Si47xx Baseboard Rev1.3 - Bill of Materials,” on page 51 and Table 9, “Si471x-EVB Daughter Card Rev1.2 - Bill of Materials,” on page 53.

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NOTES:

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CONTACT INFORMATION

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: FMinfo@silabs.com
Internet: www.silabs.com

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